

OLED DISPLAY MODULE

Product Specification

| | | |
|--------------------------|----------------------|-------------|
| CUSTOMER | Standard | |
| PRODUCT NUMBER | DD-12832BE-1B | |
| CUSTOMER APPROVAL | | Date |

| INTERNAL APPROVALS | | |
|------------------------|------------------------|---------------------|
| Product Mgr | Doc. Control | Electr. Eng |
| Bruno Recaldini | Anthony Perkins | SZU WEI CHEN |
| Date: 18 Nov 13 | Date: 18 Nov 13 | Date: 18 Nov 13 |

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REVISION RECORD



| Rev. | Date | Page | Chapt. | Comment | ECR no. |
|------|-----------|------|--------|--|---------|
| A | 18 Nov 13 | | | Upgraded model from DD-12832BE-1A <ul style="list-style-type: none"> • SSD1305→SSD1309 • Improved Operation and storage temperature range • Improved life time • Revised ICC current • Timing characteristics • SW register setting • Packaging | |
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1 MAIN FEATURES

| ITEM | CONTENTS |
|-----------------------|-------------------------|
| Display Format | 128 x 32 Dots |
| Overall Dimensions | 62.00 x 24.00 x 2.00 mm |
| Colour | Monochrome (Light Blue) |
| Active Area | 55.02 x 13.10 mm |
| Viewing Area | 57.02 x 15.1 mm |
| Display Mode | Passive Matrix (2.23") |
| Driving Method | 1/32 duty |
| Driver IC | SSD1309 |
| Operating temperature | -40 ~ +85 |
| Storage temperature | -40 ~ +90 |

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2 MECHANICAL SPECIFICATION

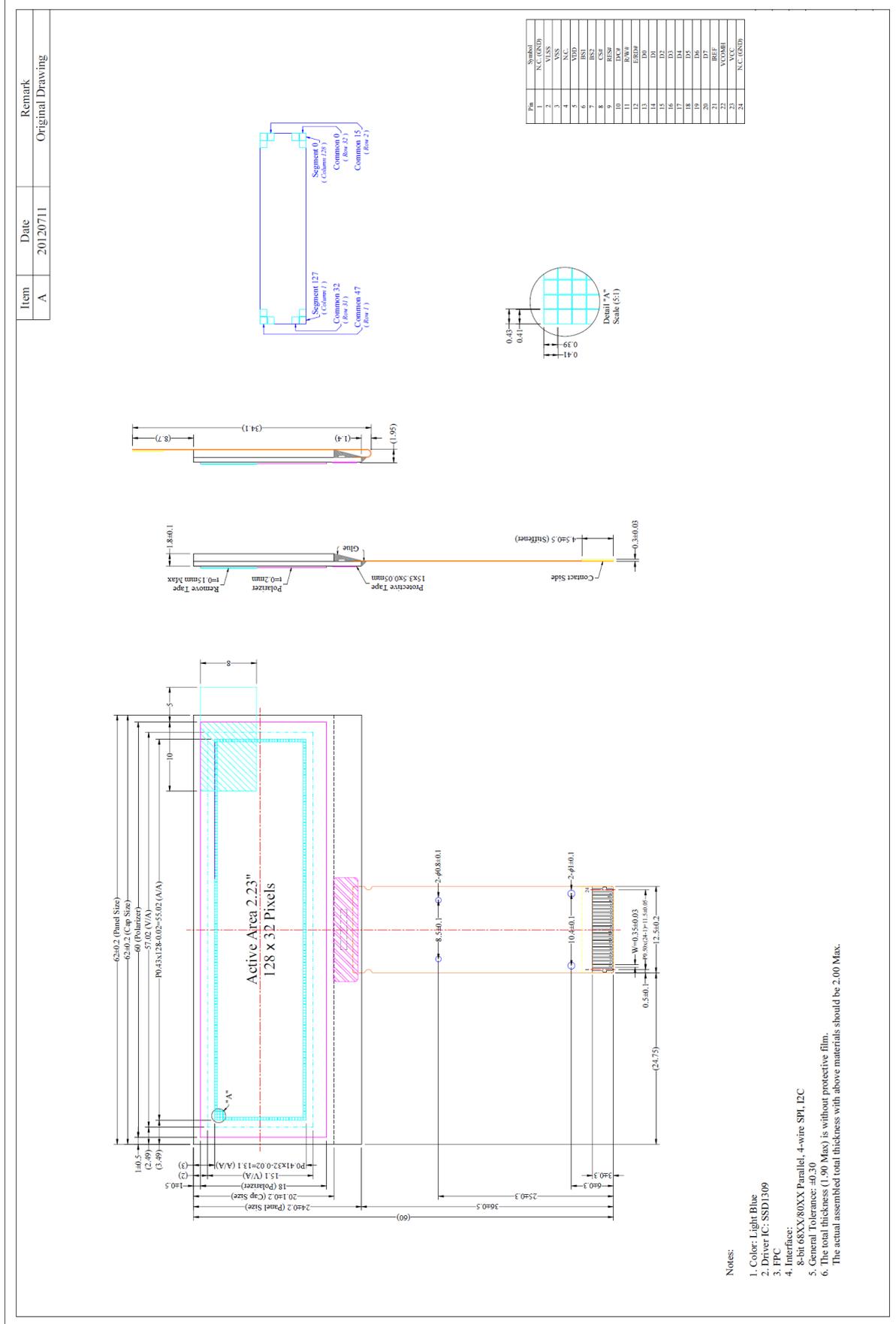
2.1 MECHANICAL CHARACTERISTICS

| ITEM | CHARACTERISTIC | UNIT |
|----------------------|----------------------|------|
| Display Format | 128 x 32 Dots | Dots |
| Overall Dimensions | 62.00 x 24.00 x 2.00 | mm |
| Active Area | 55.02 x 13.10 | mm |
| Dot Size | 0.41 x 0.39 | mm |
| Dot Pitch | 0.43 x 0.41 | mm |
| Weight | 5.82 ±10% | g |
| IC Controller/Driver | SSD1309 | |

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2.2 MECHANICAL DRAWING



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3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Min | Max | Unit | Note |
|------------------------------------|---|--------|-----|------|------|
| Supply Voltage for logic | V _{DD} | -0.3 | 4.0 | V | 1, 2 |
| Supply voltage for Display | V _{CC} | 0 | 15 | V | |
| Operating Temperature | Top | -40 | 85 | °C | 3 |
| Storage Temperature | Tst | -40 | 90 | °C | 3 |
| Life time (120 cd/m ²) | | 8,000 | - | Hour | 4 |
| Life time (80 cd/m ²) | | 15,000 | - | Hour | 4 |
| Life time (60 cd/m ²) | | 25,000 | - | Hour | 4 |
| Static Electricity | Be sure that you are grounded when handling displays. | | | | |

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: VCC = 12.5V, Ta = 25°C, 50% Checkerboard. Software configuration follows Section 5.4 Initialization. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

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3.2 ELECTRICAL CHARACTERISTICS

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-----------------------|------------------------------------|-----------------------|------|-----------------------|------|
| Supply Voltage | V _{DD} | | 1.65 | 2.8 | 3.3 | V |
| Supply Voltage for Display | V _{CC} | Note 5 | 12 | 12.5 | 13.0 | V |
| High Level Input | V _{IH} | I _{OUT} =0.1mA, 3.3MHz | 0.8xV _{DD} | - | V _{DD} | V |
| Low Level Input | V _{IL} | | 0 | - | 0.2 x V _{DD} | V |
| High Level Output | V _{OH} | | 0.9 x V _{DD} | - | V _{DD} | V |
| Low Level Output | V _{OL} | | 0 | - | 0.1 x V _{DD} | V |
| Operating current for V _{DD} | I _{DD} | | - | 180 | 300 | μA |
| Operating current for V _{CC} | I _{CC} | Note 6 | - | 10.2 | 12.8 | mA |
| | | Note 7 | - | 17.0 | 21.3 | |
| | | Note 8 | - | 32.7 | 40.9 | |
| Sleep mode current for V _{DD} | I _{DD SLEEP} | | - | 1 | 5 | μA |
| Sleep mode current for V _{CC} | I _{CC SLEEP} | | - | 2 | 10 | μA |

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 6: V_{DD} = 2.8V, V_{CC} = 12.5V, 30% Display Area Turn on.

Note 7: V_{DD} = 2.8V, V_{CC} = 12.5V, 50% Display Area Turn on.

Note 8: V_{DD} = 2.8V, V_{CC} = 12.5V, 100% Display Area Turn on.

*Software configuration follows Section 5.4 Initialization.

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3.3 INTERFACE PIN ASSIGNMENT

| No. | Symbol | Function | | | | | | | | | | | | | | | |
|---------------------|-----------|---|--|-----|-----|------------------|---|---|---------------|---|---|---------------------|---|---|---------------------|---|---|
| 1,24 | N.C.(GND) | Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit. | | | | | | | | | | | | | | | |
| 2 | VLSS | Ground of Analog Circuit This is an analog ground pin. It should be connected to VSS externally | | | | | | | | | | | | | | | |
| 3 | VSS | Ground of OEL System This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground. | | | | | | | | | | | | | | | |
| 4 | N.C. | No Connection | | | | | | | | | | | | | | | |
| 5 | VDD | Power Supply for Logic Circuit This is a voltage supply pin. It must be connected to external source. | | | | | | | | | | | | | | | |
| 6 | BS1 | Communicating Protocol Select These pins are MCU interface selection input. See the following table: | | | | | | | | | | | | | | | |
| 7 | BS2 | <table border="1"> <thead> <tr> <th></th> <th>BS1</th> <th>BS2</th> </tr> </thead> <tbody> <tr> <td>I²C</td> <td>1</td> <td>0</td> </tr> <tr> <td>4-wire Serial</td> <td>0</td> <td>0</td> </tr> <tr> <td>8-bit 68XX Parallel</td> <td>0</td> <td>1</td> </tr> <tr> <td>8-bit 80XX Parallel</td> <td>1</td> <td>1</td> </tr> </tbody> </table> | | BS1 | BS2 | I ² C | 1 | 0 | 4-wire Serial | 0 | 0 | 8-bit 68XX Parallel | 0 | 1 | 8-bit 80XX Parallel | 1 | 1 |
| | BS1 | BS2 | | | | | | | | | | | | | | | |
| I ² C | 1 | 0 | | | | | | | | | | | | | | | |
| 4-wire Serial | 0 | 0 | | | | | | | | | | | | | | | |
| 8-bit 68XX Parallel | 0 | 1 | | | | | | | | | | | | | | | |
| 8-bit 80XX Parallel | 1 | 1 | | | | | | | | | | | | | | | |
| 8 | CS# | Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low. | | | | | | | | | | | | | | | |
| 9 | RES# | Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. | | | | | | | | | | | | | | | |
| 10 | D/C# | Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection. | | | | | | | | | | | | | | | |
| 11 | R/W# | Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. | | | | | | | | | | | | | | | |
| 12 | E/RD# | Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. | | | | | | | | | | | | | | | |
| 13~20 | D0~D7 | Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the | | | | | | | | | | | | | | | |

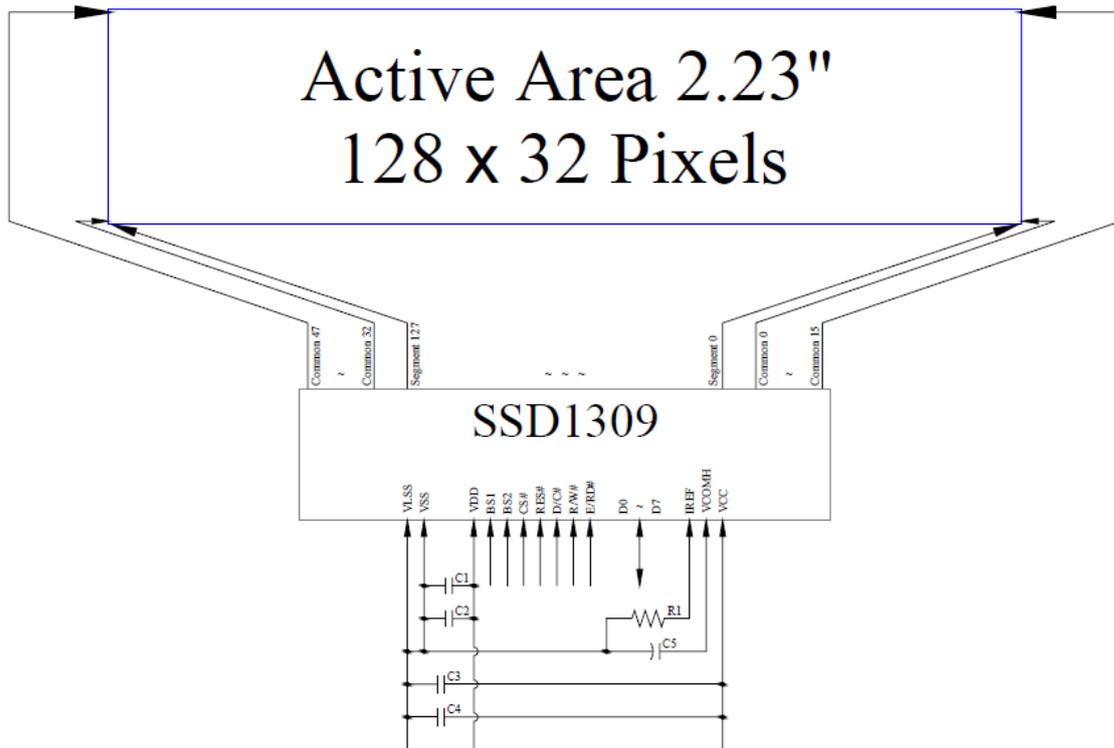
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| | | <p>microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tied together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.</p> <p>Unused pins must be connected to Vss except for D2 in serial mode.</p> |
| 21 | IREF | <p>Current Reference for Brightness Adjustment</p> <p>This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA</p> |
| 22 | VCOMH | <p>Voltage Output High Level for COM signal</p> <p>This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.</p> |
| 23 | VCC | <p>Power Supply for OEL Panel</p> <p>This is the most positive voltage supply pin of the chip. It must be supplied externally.</p> |
| 24 | N.C.(GND) | <p>Reserved Pin (Supporting Pin)</p> <p>The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.</p> |

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3.4 BLOCK DIAGRAM



MCU Interface Selection: BS1 and BS2

Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, RES# and CS#.

C1, C3: 0.1µF

C2: 4.7µF

C4: 10µF

C5: 4.7µF/25V Tantalum Capacitor

R1: 910 kΩ, $R1 = (\text{Voltage at IREF} - VSS) / IREF$

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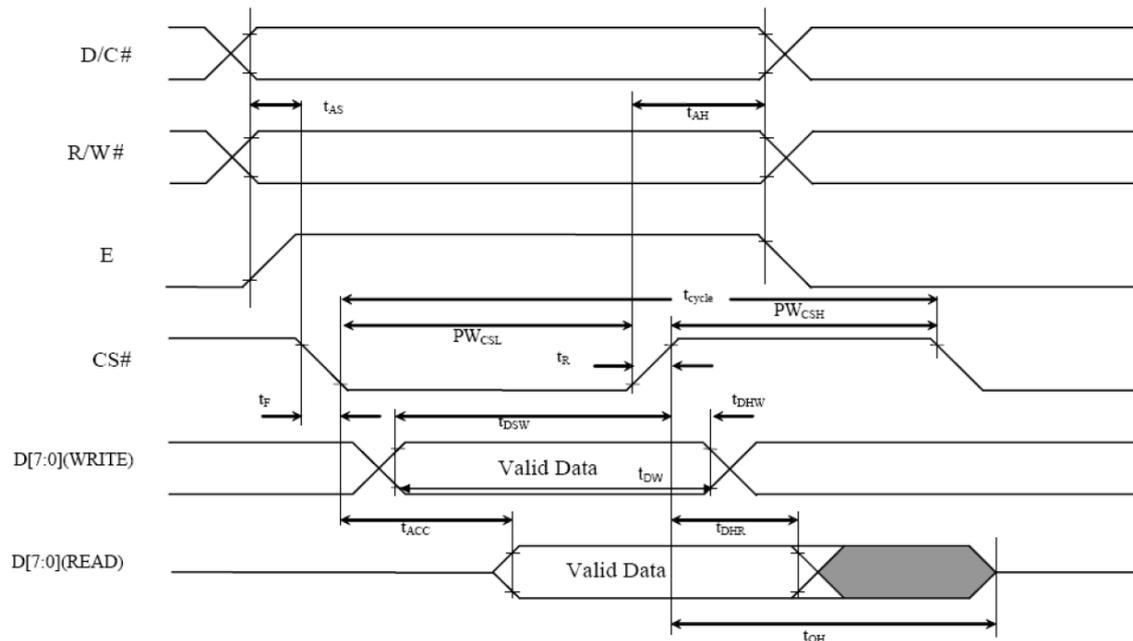
3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

3.5.1.1 68XX-Series MPU Parallel Interface Timing Characteristics

$V_{DD}-V_{SS} = 2.4V$ to $3.5V$, $T_a=25^{\circ}C$

| Symbol | Description | Min | Max | Unit |
|--------------------|---|-----|-----|------|
| t _{cycle} | System Cycle Time | 300 | - | ns |
| t _{AS} | Address Setup Time | 20 | - | ns |
| t _{AH} | Address Hold Time | 0 | - | ns |
| t _{DW} | Data Write Time | 80 | - | ns |
| t _{DSW} | Write Data Setup Time | 40 | - | ns |
| t _{DHW} | Write Data Hold Time | 20 | - | ns |
| t _{DHR} | Read Data Hold Time | 20 | - | ns |
| t _{OH} | Output Disable Time | - | 70 | ns |
| t _{ACC} | Access Time | - | 140 | ns |
| PW _{CSL} | Chip Select Low Pulse Width (Read) Chip Select | 120 | - | ns |
| | Low Pulse width (Write) | 60 | | |
| PW _{CSH} | Chip Select High Pulse Width (Read) Chip Select | 60 | - | ns |
| | High Pulse Width (Write) | 60 | | |
| t _R | Rise Time | - | 40 | ns |
| t _F | Fall Time | - | 40 | ns |



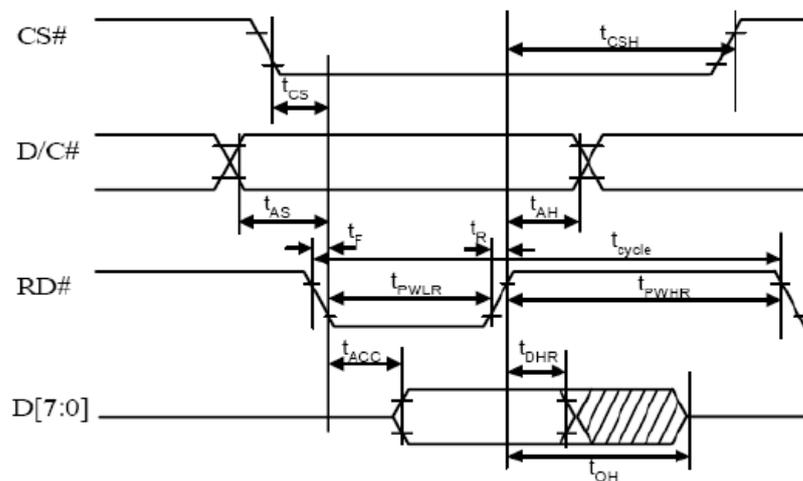
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3.5.1.2 80XX-Series MPU Parallel Interface Timing Characteristics

$V_{DD}-V_{SS} = 1.65V$ to $3.3V$, $T_a=25^{\circ}C$

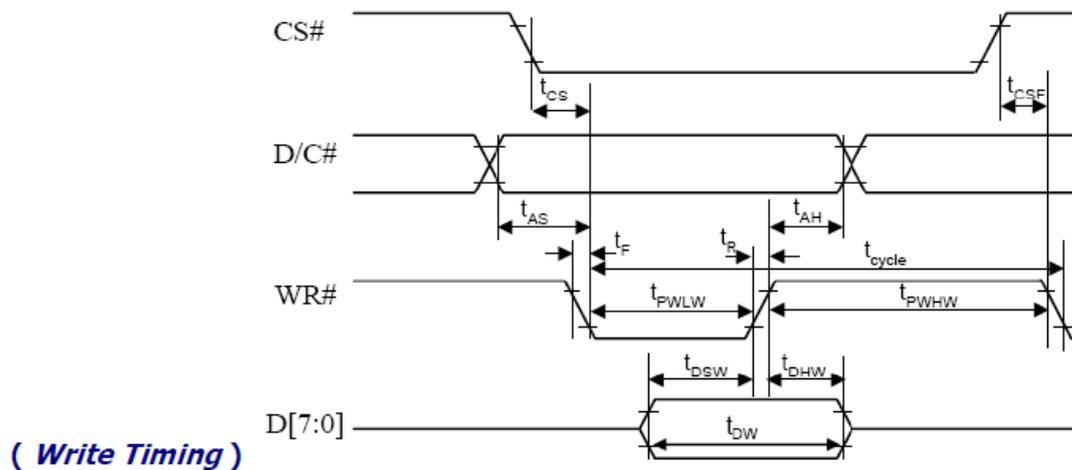
| Symbol | Description | Min | Max | Unit |
|--------------------|--------------------------------------|-----|-----|------|
| t _{cycle} | Clock Cycle Time | 300 | - | ns |
| t _{AS} | Address Setup Time | 20 | - | ns |
| t _{AH} | Address Hold Time | 0 | - | ns |
| t _{DW} | Data Write Time | 70 | - | ns |
| t _{DSW} | Write Data Setup Time | 40 | - | ns |
| t _{DHW} | Write Data Hold Time | 15 | - | ns |
| t _{DHR} | Read Data Hold Time | 20 | - | ns |
| t _{OH} | Output Disable Time | - | 70 | ns |
| t _{ACC} | Access Time | - | 140 | ns |
| t _{PWLR} | Read Low Time | 120 | - | ns |
| t _{PWLW} | Write Low Time | 60 | - | ns |
| t _{PWHR} | Read High Time | 60 | - | ns |
| t _{PHW} | Write High Time | 60 | - | ns |
| t _{CS} | Chip Select Setup Time | 0 | - | ns |
| t _{CSH} | Chip Select Hold Time to Read Signal | 0 | - | ns |
| t _{CSF} | Chip Select Hold Time | 20 | - | ns |
| t _R | Rise Time | - | 40 | ns |
| t _F | Fall Time | - | 40 | ns |



(Read Timing)

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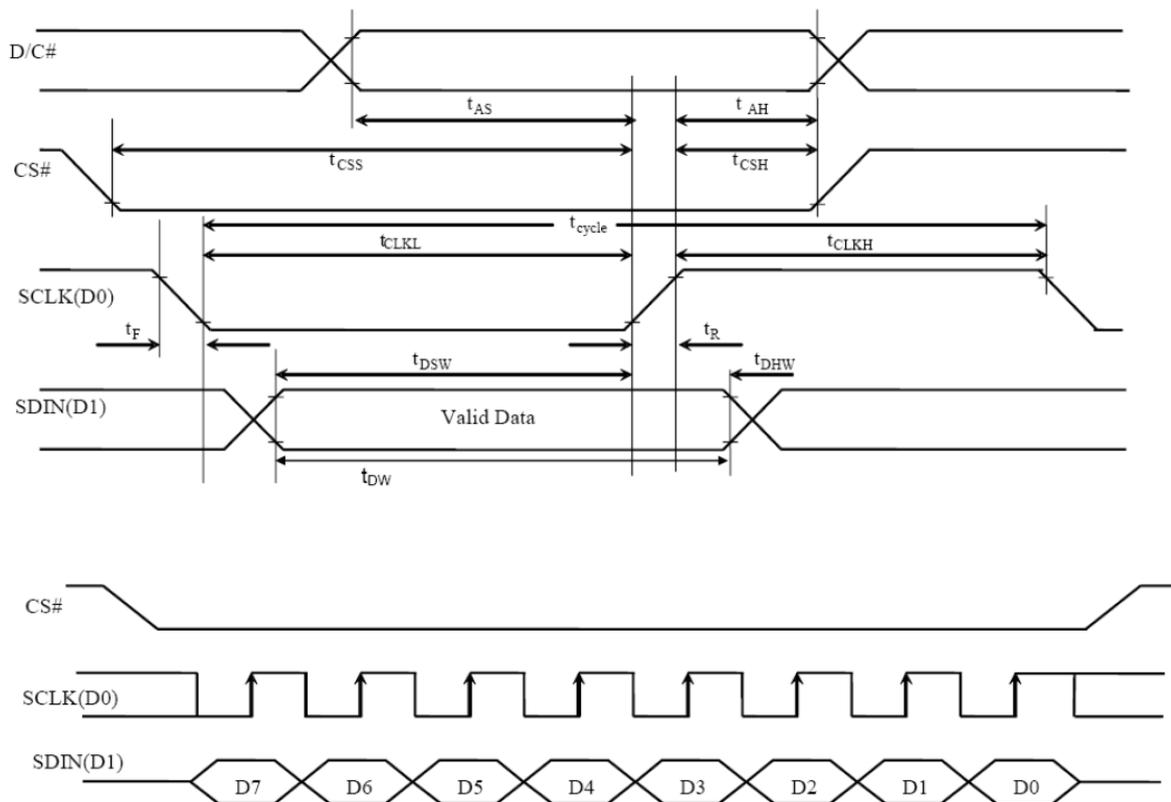
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3.5.1.3 Serial Interface Timing Characteristics

$V_{DD}-V_{SS} = 1.65V$ to $3.3V$, $T_a=25^{\circ}C$

| Symbol | Description | Min | Max | Unit |
|--------------------|------------------------|-----|-----|------|
| t _{cycle} | Clock Cycle Time | 100 | - | ns |
| t _{AS} | Address Setup Time | 15 | - | ns |
| t _{AH} | Address Hold Time | 15 | - | ns |
| t _{CSS} | Chip Select Setup Time | 20 | - | ns |
| t _{CSH} | Chip Select Hold Time | 50 | - | ns |
| t _{DW} | Data Write Time | 55 | - | ns |
| t _{DSW} | Write Data Setup Time | 15 | - | ns |
| t _{DHW} | Write Data Hold Time | 15 | - | ns |
| t _{CLKL} | Serial Clock Low Time | 50 | - | ns |
| t _{CLKH} | Serial Clock High Time | 50 | - | ns |
| t _R | Rise Time | - | 40 | ns |
| t _F | Fall Time | - | 40 | ns |



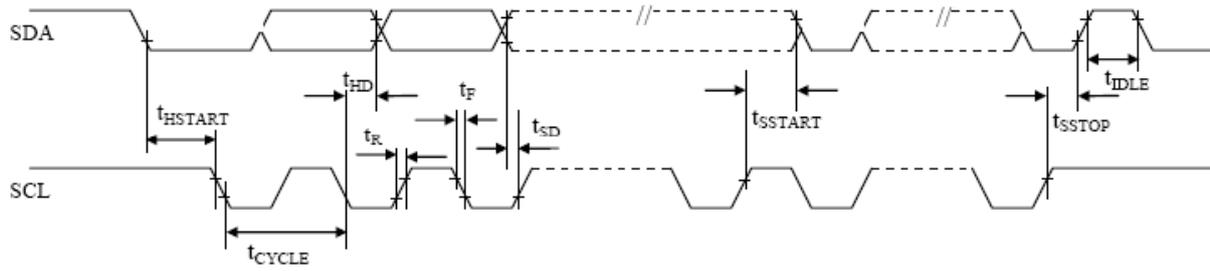
3.5.1.4 I²C Interface Timing Characteristics

$V_{DD}-V_{SS} = 1.65V$ to $3.3V$, $T_a=25^{\circ}C$

| Symbol | Description | Min | Max | Unit |
|--------------|--|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 2.5 | - | us |
| t_{HSTART} | Start Condition Hold Time | 0.6 | - | us |
| t_{HD} | Data Hold Time (for "SDAOUT" Pin) Data | 0 | - | ns |
| | Hold Time (for "SDAIN" Pin) | 300 | | |
| t_{SD} | Data Setup Time | 100 | - | ns |
| t_{SSTART} | Start Condition Setup Time (Only relevant for a repeated Start condition) | 0.6 | - | us |
| t_{SSTOP} | Stop Condition Setup Time | 0.6 | - | us |
| t_R | Rise Time for Data and Clock Pin | | 300 | ns |
| t_F | Fall Time for Data and Clock Pin | | 300 | ns |
| t_{IDLE} | Idle Time before a New Transmission can Start | 1.3 | - | us |

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4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

| Characteristics | Symbol | Condition | Min | Typ | Max | Unit |
|--------------------|-----------------|--------------------------------------|------|-----------|------|-------------------|
| Brightness(White) | L _{br} | With polarizer (Note 5 on page 8) | 100 | 120 | - | cd/m ² |
| C.I.E.(Blue) | (X) | Without polarizer | 0.12 | 0.16 | 0.20 | - |
| | (Y) | | 0.22 | 0.26 | 0.30 | |
| Dark Room Contrast | CR | | - | >10,000:1 | - | - |
| Viewing Angle | | | - | Free | - | degree |

Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12.5V.
Software configuration follows Section 5.4 Initialization

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5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

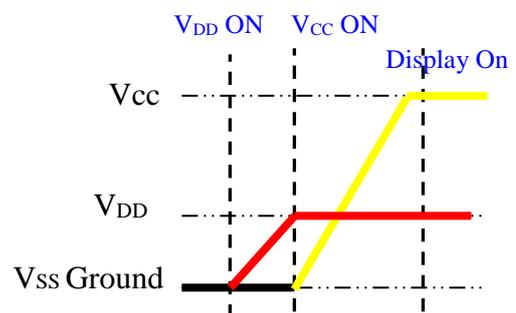
Please refer to the Technical Manual for the SSD1309

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

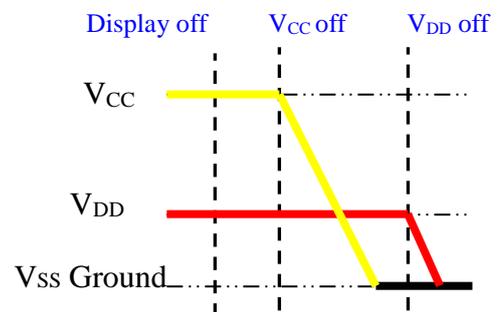
5.2.1 POWER UP SEQUENCE

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(when V_{CC} is stable)
7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
(When V_{CC} reach 0 and panel is completely discharges)
4. Power down V_{DD}



5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128x64 Display mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80h
9. Normal display mode (Equivalent to A4h command)

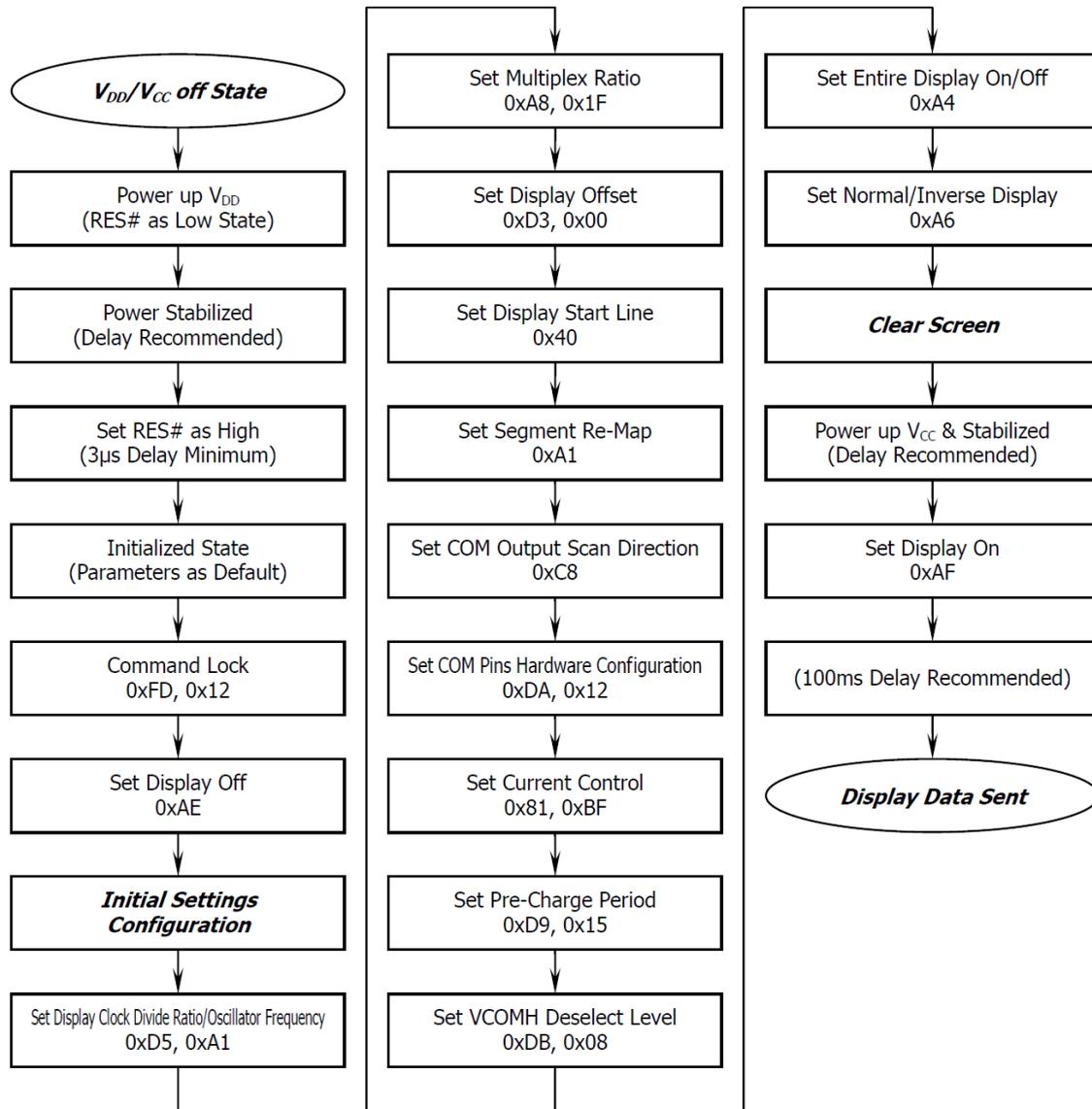
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5.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example

<Power up Sequence>

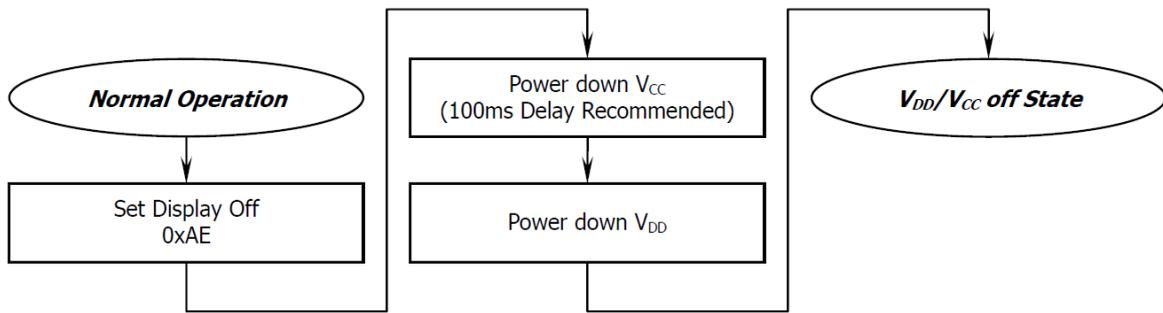


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

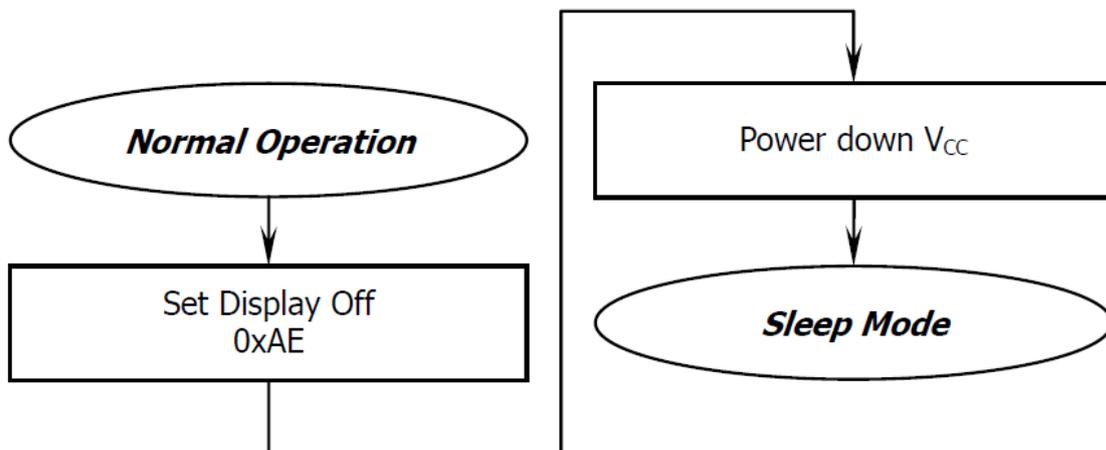
<Power down Sequence>

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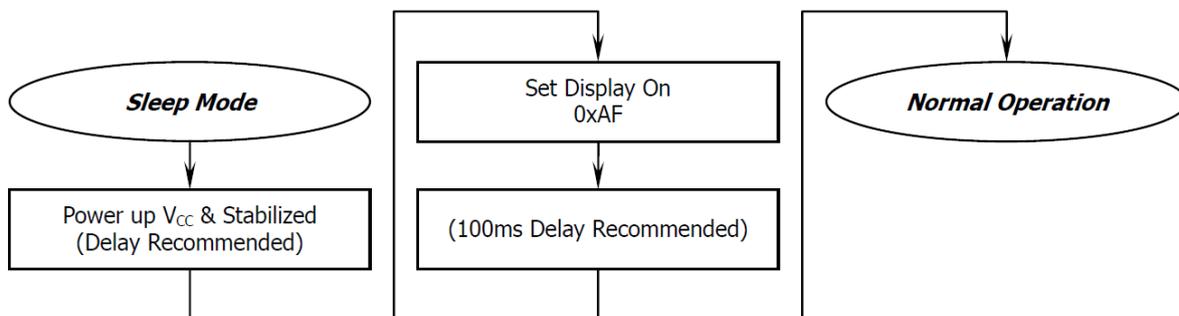
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<Entering Sleep Mode>



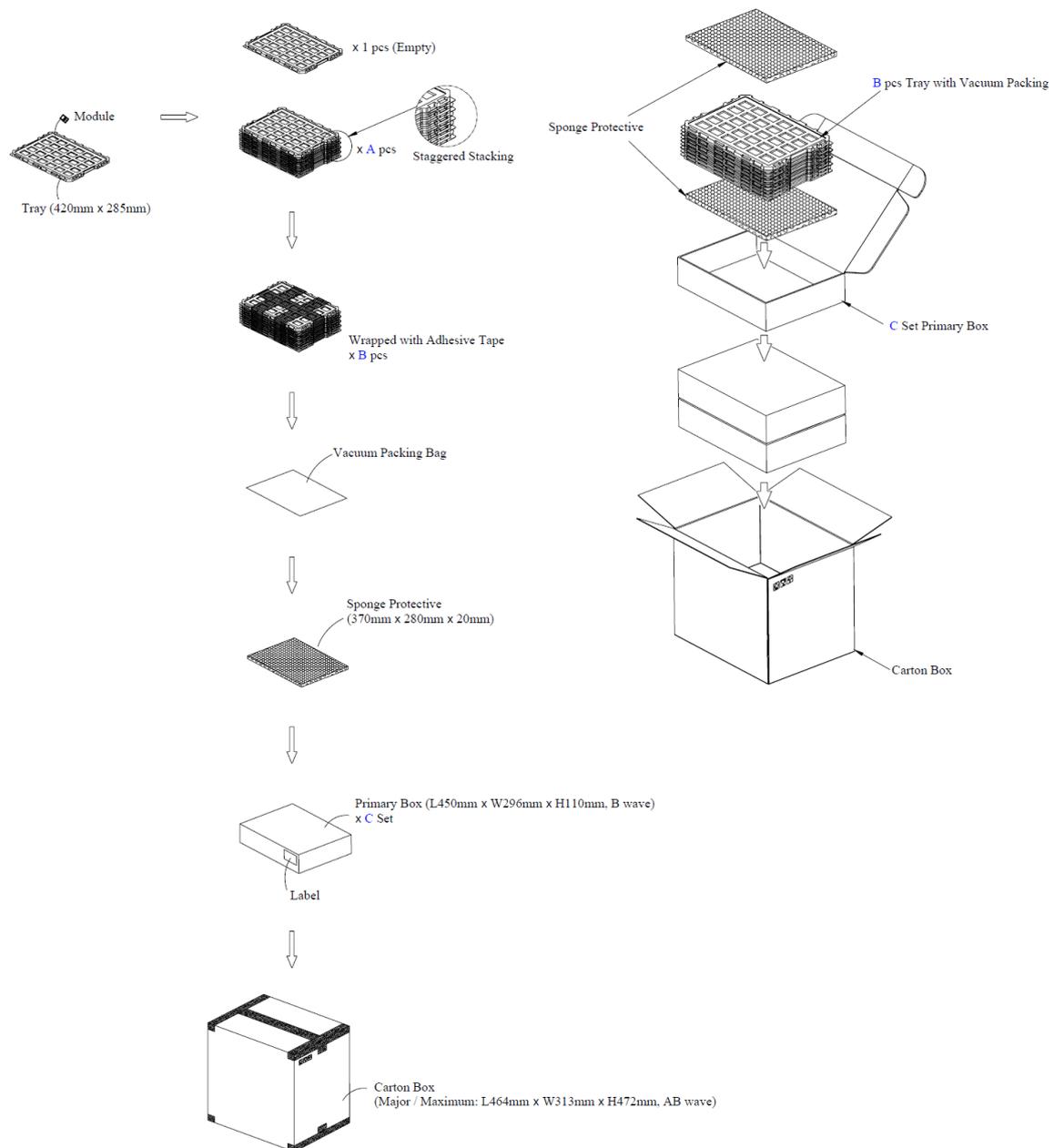
<Exiting Sleep Mode>



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6 PACKAGING AND LABELLING SPECIFICATION



| Item | Quantity | |
|--------------------------|------------|---|
| Module | 225 | per Primary Box |
| Holding Trays (A) | 15 | per Primary Box |
| Total Trays (B) | 16 | per Primary Box (Including 1 Empty Tray) |
| Primary Box (C) | 1~4 | per Carton (4 as Major / Maximum) |

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7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

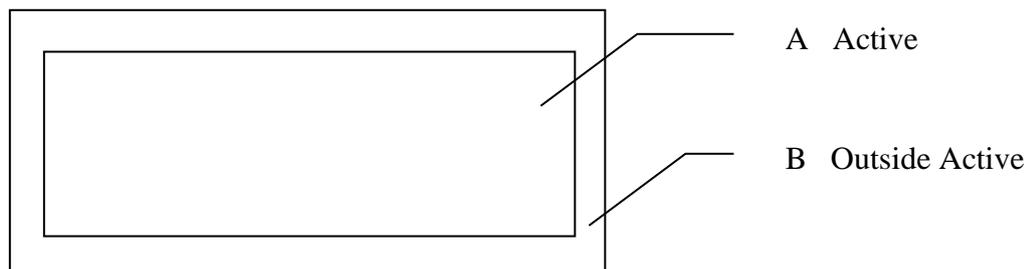
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



7.2.3 Visual inspection

Test and measurement to be conducted under following conditions:

| | |
|---|----------|
| Temperature: | 23±5°C |
| Humidity: | 55±15%RH |
| Fluorescent lamp: | 30 W |
| Distance between the Panel & Eyes of the Inspector: | ≥30cm |
| Distance between the Panel & the lamp: | ≥50cm |

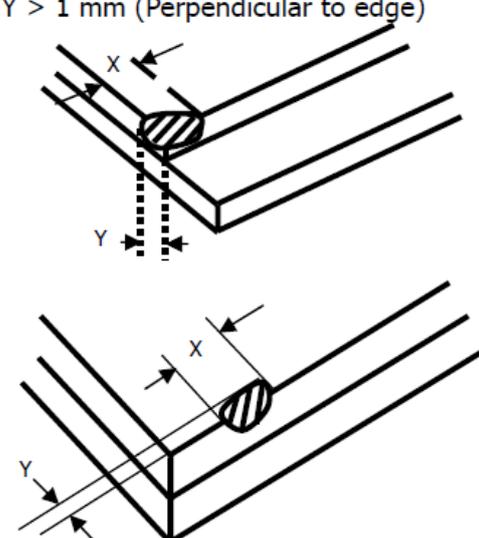
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7.2.4 Standard of appearance inspection

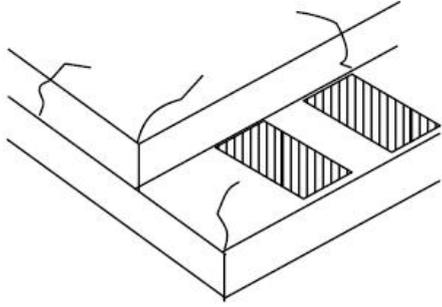
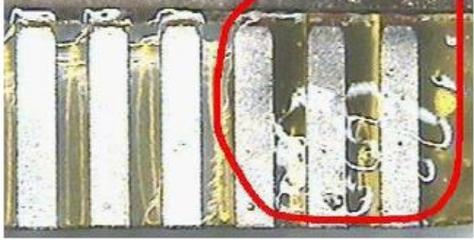
7.2.4.1 Cosmetic Check (Display Off) in Non-Active Area

| Partition | AQL | Definition |
|-----------|------|---|
| Major | 0.65 | Defects in Pattern Check (Display On) |
| Minor | 1.0 | Defects in Cosmetic Check (Display Off) |

| Check Item | Classification | Criteria |
|------------------------|----------------|--|
| Panel General Chipping | Minor | <p>X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)</p>  |

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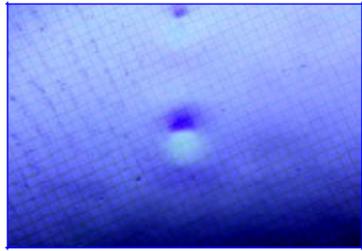
| Check Item | Classification | Criteria |
|---|----------------|---|
| Panel Crack | Minor | Any crack is not allowable.  |
| Copper Exposed (Even Pin or Film) | Minor | Not Allowable by Naked Eye Inspection |
| Film or Trace Damage | Minor |  |
| Terminal Lead Prober Mark | Acceptable |  |
| Glue or Contamination on Pin (Couldn't Be Removed by Alcohol) | Minor |  |
| Ink Marking on Back Side of panel (Exclude on Film) | Acceptable | Ignore for Any |

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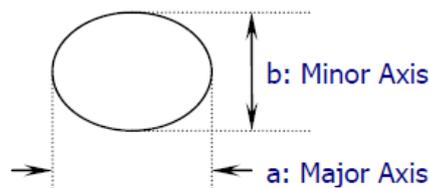
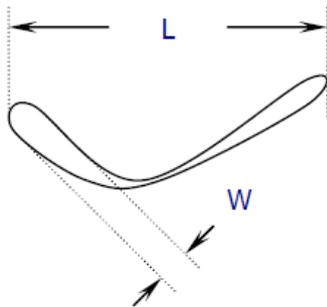
7.2.4.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary

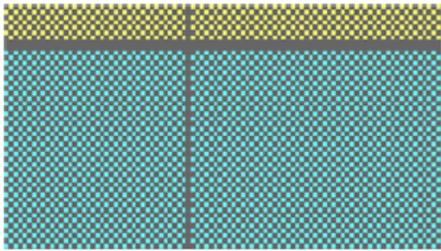
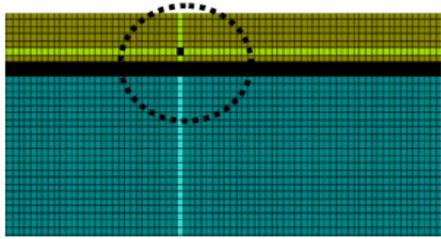
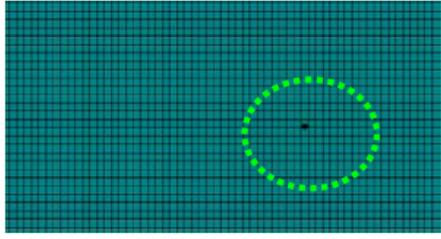
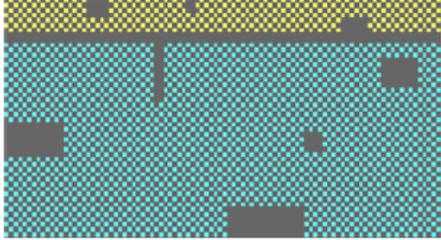
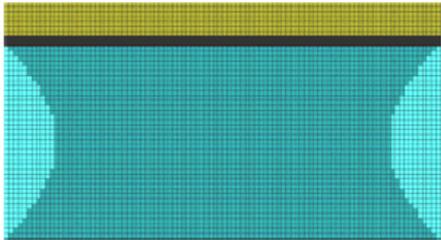
| Check Item | Classification | Criteria |
|---|----------------|---|
| Any Dirt & Scratch on Polarizer's Protective Film | Acceptable | Ignore for not Affect the Polarizer |
| Scratches, Fiber, Line-Shape Defect (On Polarizer) | Minor | $W \leq 0.1$ Ignore $W > 0.1$ $L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$ |
| Dirt, Black Spot, Foreign Material, (On Polarizer) | Minor | $\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$ |
| Dent, Bubbles, White spot (Any Transparent Spot on Polarizer) | Minor | $\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$  |
| Fingerprint, Flow Mark (On Polarizer) | Minor | Not Allowable |

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$



7.2.4.3 Pattern Check (Display On) in Active Area

| Check Item | Classification | Criteria |
|---------------|----------------|--|
| No Display | Major |  |
| Missing Line | Major |  |
| Pixel Short | Major |  |
| Darker Pixel | Major |  |
| Wrong Display | Major |  |
| Un-uniform | Major |  |

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.

After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

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8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

| Test Item | Test Condition | Evaluation and assessment |
|--|--|---|
| High Temperature Operation | 85°C, 500 hours | No abnormalities in function and appearance |
| Low Temperature Operation | -40°C, 500 hours | No abnormalities in function and appearance |
| High Temperature Storage | 90°C, 500 hours | No abnormalities in function and appearance |
| Low Temperature Storage | -40°C, 500 hours | No abnormalities in function and appearance |
| High Temperature & High Humidity Storage | 60°C, 90%RH, 240 hours | No abnormalities in function and appearance |
| Thermal Shock | 100 cycle of -40°C ↔ 85°C 30 Mins dwell | No abnormalities in function and appearance |

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5 °C; 55±15% RH

8.2 LIFE TIME

| Item | Description |
|------|--|
| 1 | Function, performance, appearance, etc. shall be free from remarkable deterioration for minimum: 8,000 hours under 120 cd/m ² brightness 15,000 hours under 80 cd/m ² brightness 25,000 hours under 60 cd/m ² brightness and 50% Checkerboard, humidity (50% RH), and in area not exposed to direct sunlight. |
| 2 | End of lifetime is specified as 50% of initial brightness. |
| 3 | Reduction in operating brightness will result in an extension of half-life. Especially when the brightness less than 80 cd/m ² , the lifetime extended more obviously. |

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9 HANDLING PRECAUTIONS

Safety

If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.

Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotrifluoroethane.

Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS} . Do not input any signals before power is turned on.

Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.

To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions

When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.

Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored.
Also, there will be no problem in the reliability of the module.

Storage

Store the display in a dark place where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the humidity below 50%RH.

Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).

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10 SUPPORTED ACCESSORIES

10.1 DUO KIT

Densitron has developed an easy to use yet powerful development and demonstration tool for driving its range of Passive Matrix OLED displays from the USB port of a PC. DUO (Densitron USB OLED) kit is hot pluggable and does not require extra cables or power supply to run, allowing users to be up and running in minutes.

The kit consists of an OLED display with transition Board, USB controller card, mini USB cable and a CD with software application and drivers.



Part number: PDK-N-12832BE-1B

10.2 TRANSITION BOARD CARD

A Transition board card is like a daughterboard which is meant to be a circuit board for connections between the baseboards (DUO).

It has connector pins for interfacing between the display and the baseboards.

It also includes the OLED display.

Part number: PDT-N-12832BE-1B

10.3 CONNECTOR BOARD CARD

A Connector board card is also a daughterboard which is a circuit board for connection between a microprocessor or microcontroller (customer's system).

Part number: EVK-CONNECT-015

10.4 CONNECTOR

Type: ZIF connector

| No. of connections | Pitch (mm) | Manufacturer | Manufacturer part no. | Distributor part no. |
|--------------------|------------|--------------|-----------------------|--|
| 24 | 0.50 | Omron | XF2M-2415-1A | Farnell-1112559 Digikey/ OR721CT-ND |

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