OLED DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-12832WE-1B**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bruno Recaldini	**Richard Applin**	**SZU WEI CHEN**
Date: 18 Nov 13	Date: 18 Nov 13	Date: 18 Nov 13

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Rev.	Date	Page	Chapt.	Comment	ECR no.
A	18 Nov 13			Upgraded model from DD-12832WE-1A • SSD1305→SSD1309 • Improved Operation and storage temperature range • Improved life time • Revised ICC current • Timing characteristics • SW register setting • Packaging	

1 MAIN FEATURES

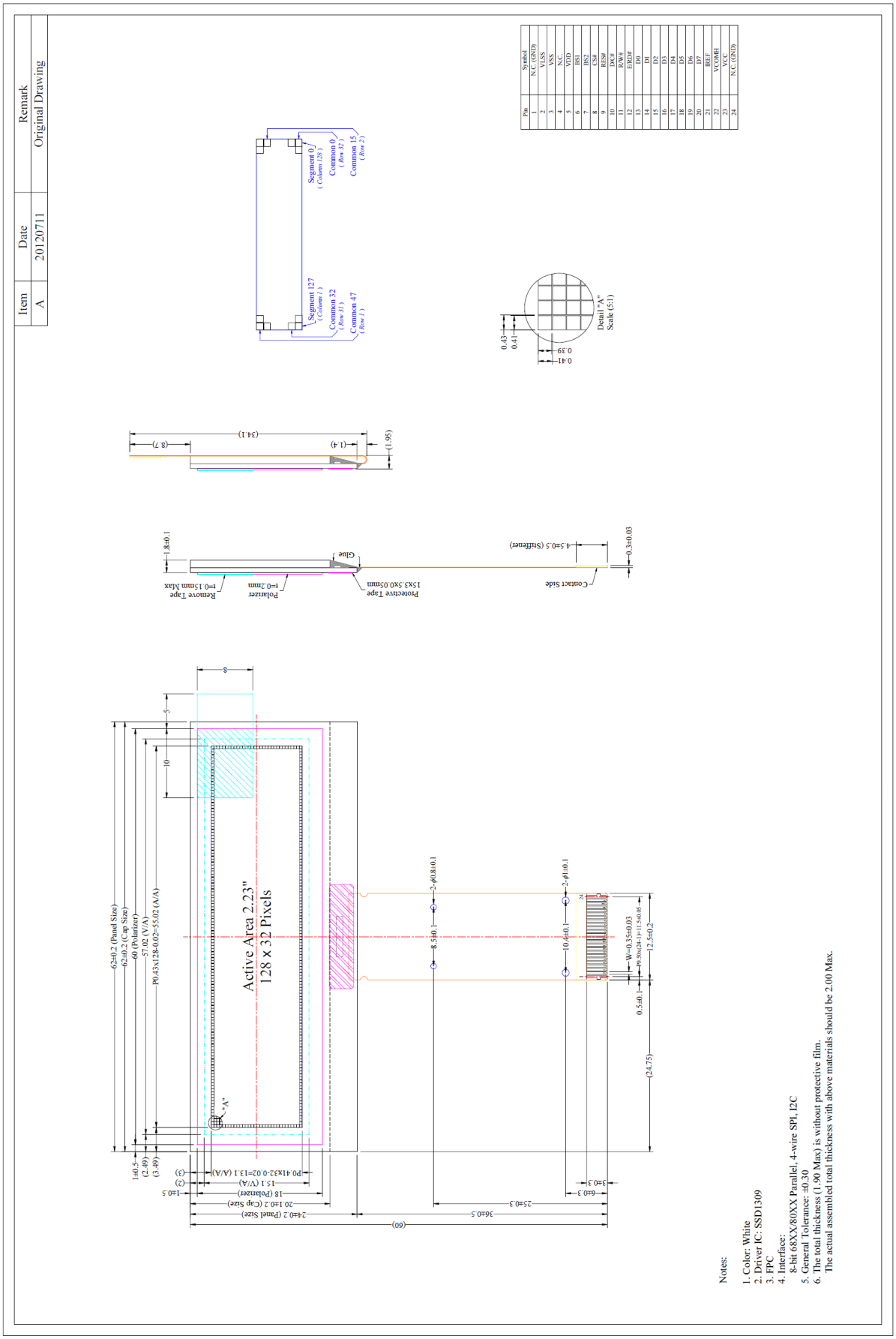
ITEM	CONTENTS
Display Format	128 x 32 Dots
Overall Dimensions	62.00 x 24.00 x 2.00 mm
Colour	Monochrome White
Active Area	55.02 x 13.10 mm
Display Mode	Passive Matrix (2.23”)
Driving Method	1/32 duty
Driver IC	SSD1309
Operating temperature	-40 ~ +85
Storage temperature	-40 ~ +90

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	128 x 32 Dots	Dots
Overall Dimensions	62.00 x 24.00 x 2.00	mm
Active Area	55.02 x 13.10	mm
Dot Size	0.41 x 0.39	mm
Dot Pitch	0.43 x 0.41	mm
Weight	5.82±10%	g
IC Controller/Driver	SSD1309	

2.2 MECHANICAL DRAWING



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3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for logic	V_{DD}	-0.3	4.0	V	1, 2
Supply voltage for Display	V_{CC}	0	15	V	
Operating Temperature	Top	-40	85	°C	3
Storage Temperature	Tstg	-40	90	°C	3
Life Time (120 cd/m^2)		10,000	-	Hour	4
Life Time (80 cd/m^2)		30,000	-	Hour	4
Life Time (60 cd/m^2)		50,000	-	Hour	4
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: VCC = 12.5V, Ta = 25°C, 50% Checkerboard. Software configuration follows Section 5.4 Initialization. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display	V_{CC}	Note 5	12	12.5	13.0	V
High Level Input	V_{IH}	I_{OUT}=0.1mA , 3.3MHz	0.8xV_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	0.2 x V_{DD}	V
High Level Output	V_{OH}		0.9 x V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}		0	-	0.1 x V_{DD}	V
Operating current for V_{DD}	I_{DD}		-	180	300	µA
Operating current for V_{CC}	I_{CC}	Note 6	-	12.0	15.0	mA
		Note 7		19.9	24.9	
		Note 8		37.9	47.4	
Sleep mode current for V_{DD}	$I_{DD\ SLEEP}$		-	1	5	µA
Sleep mode current for V_{CC}	$I_{CC\ SLEEP}$		-	2	10	µA

Note 5: Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer's request.
Note 6: VDD = 2.8V, VCC = 12.5V, 30% Display Area Turn on.
Note 7: VDD = 2.8V, VCC = 12.5V, 50% Display Area Turn on.
Note 8: VDD = 2.8V, VCC = 12.5V, 100% Display Area Turn on.

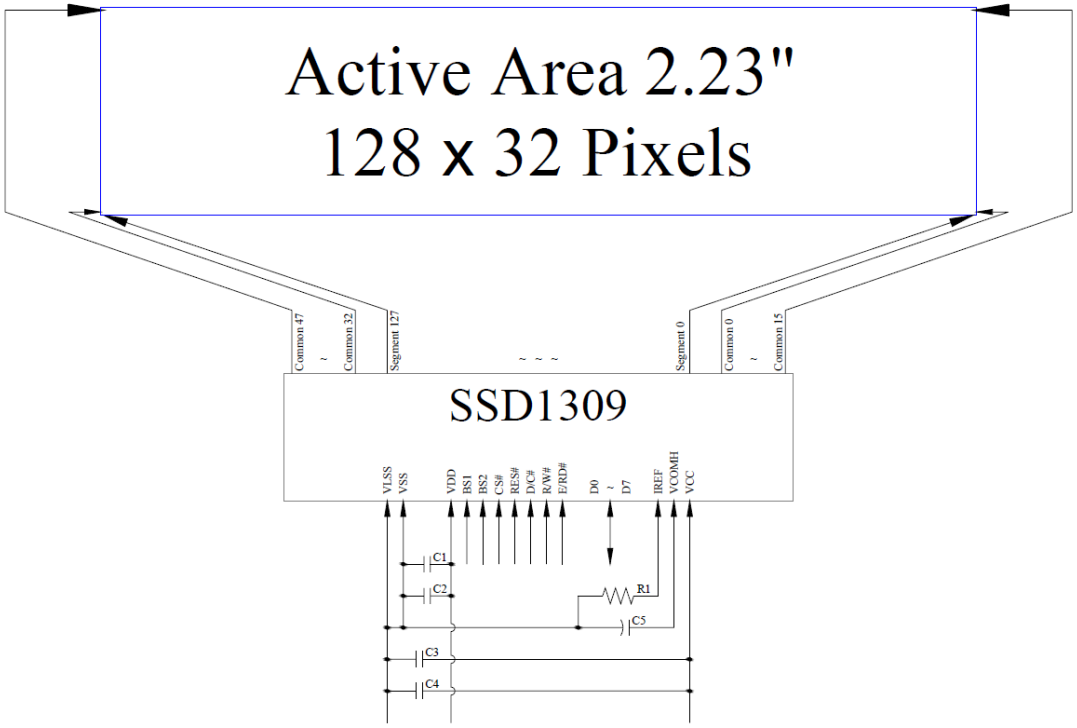
*Software configuration follows Section 5.4 Initialization

3.3 INTERFACE PIN ASSIGNMENT

<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>N.C.(GND)</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.</td></tr>
<tr><td>2</td><td>VLSS</td><td>Ground of Analog Circuit
This is an analog ground pin. It should be connected to VSS externally</td></tr>
<tr><td>3</td><td>VSS</td><td>Ground of OEL System
This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.</td></tr>
<tr><td>4</td><td>N.C.</td><td>No Connection</td></tr>
<tr><td>5</td><td>VDD</td><td>Power Supply for Logic Circuit
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>6</td><td>BS1</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table><tr><th></th><th>BS1</th><th>BS2</th></tr><tr><td>I²C</td><td>1</td><td>0</td></tr><tr><td>4-wire Serial</td><td>0</td><td>0</td></tr><tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr><tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>7</td><td>BS2</td></tr>
<tr><td>8</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>9</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>10</td><td>D/C#</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>11</td><td>R/W#</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.</td></tr>
<tr><td>12</td><td>E/RD#</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.</td></tr>
</table>

13~20	D0~D7	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tied together and serve as SDAout &SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to Vss except for D2 in serial mode.
21	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA
22	VCOMH	Voltage Output High Level for COM signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
23	VCC	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be supplied externally.
24	N.C.(GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

3.4 BLOCK DIAGRAM



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, RES# and CS#.

C1, C3: 0.1µF
C2: 4.7µF
C4: 10µF
C5: 4.7µF/25V Tantalum Capacitor
R1: 910 kΩ, R1 = (Voltage at IREF – VSS) / IREF

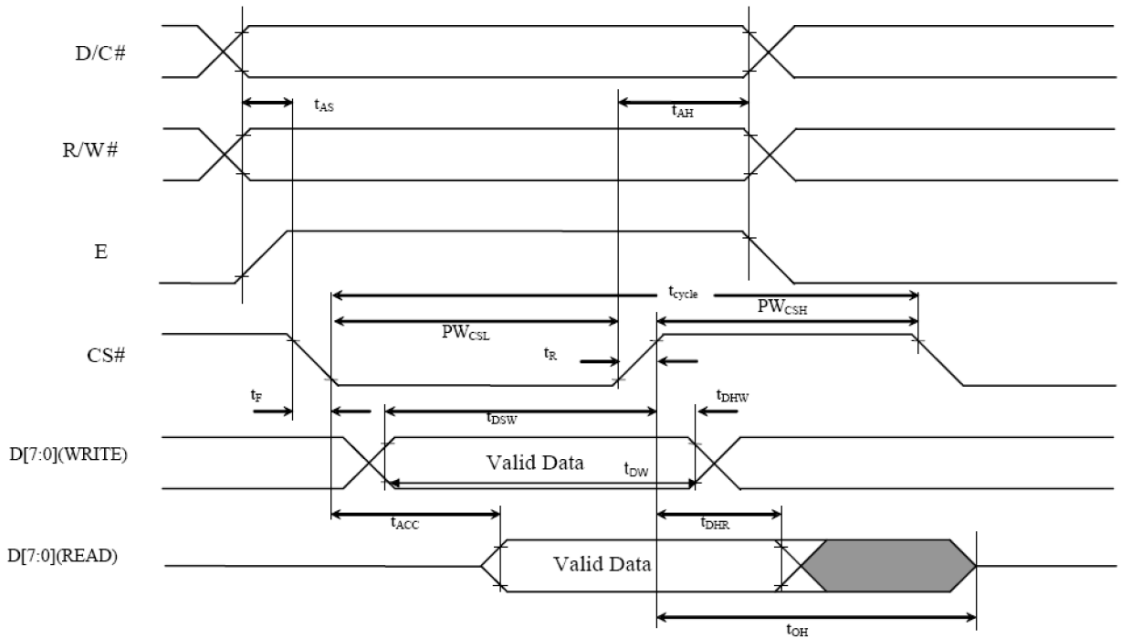
3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

3.5.1.1 68XX-Series MPU Parallel Interface Timing Characteristics

V_{DD}-V_{SS} = 1.65V to 3.3V, Ta=25ºC

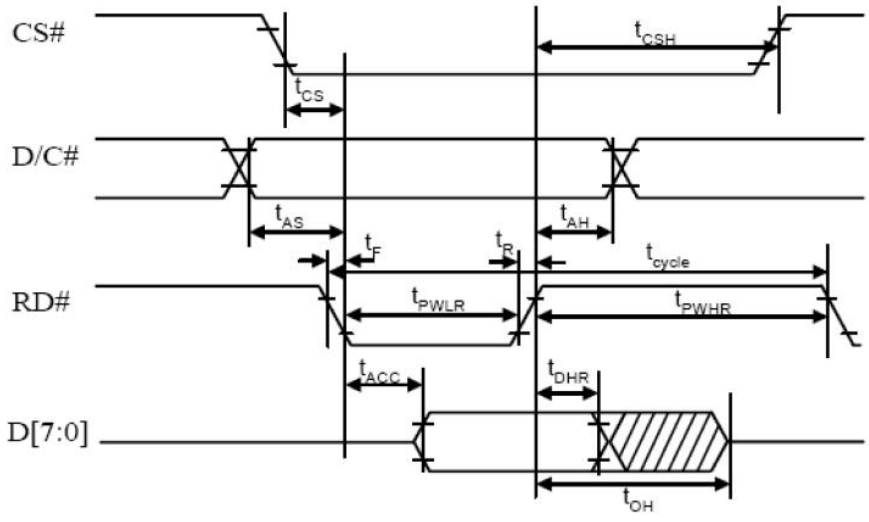
Symbol	Description	Min	Max	Unit
tcycle	System Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
tDW	Data Write Time	80	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select	120	-	ns
	Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select	60	-	ns
	High Pulse Width (Write)	60		
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns



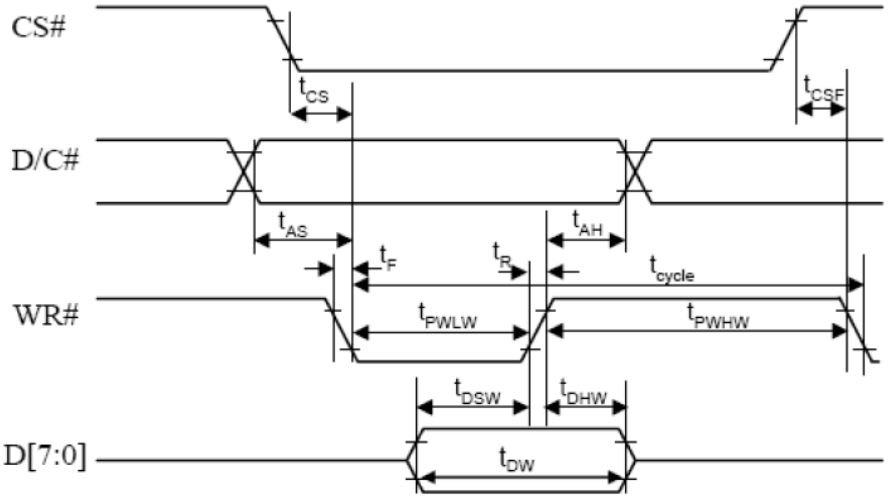
3.5.1.2 8080-Series MPU Parallel Interface Timing Characteristics

V_{DD}-V_{SS} = 1.65V to 3.3V, Ta=25°C

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
tDW	Data Write Time	70	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns



(*Read Timing*)

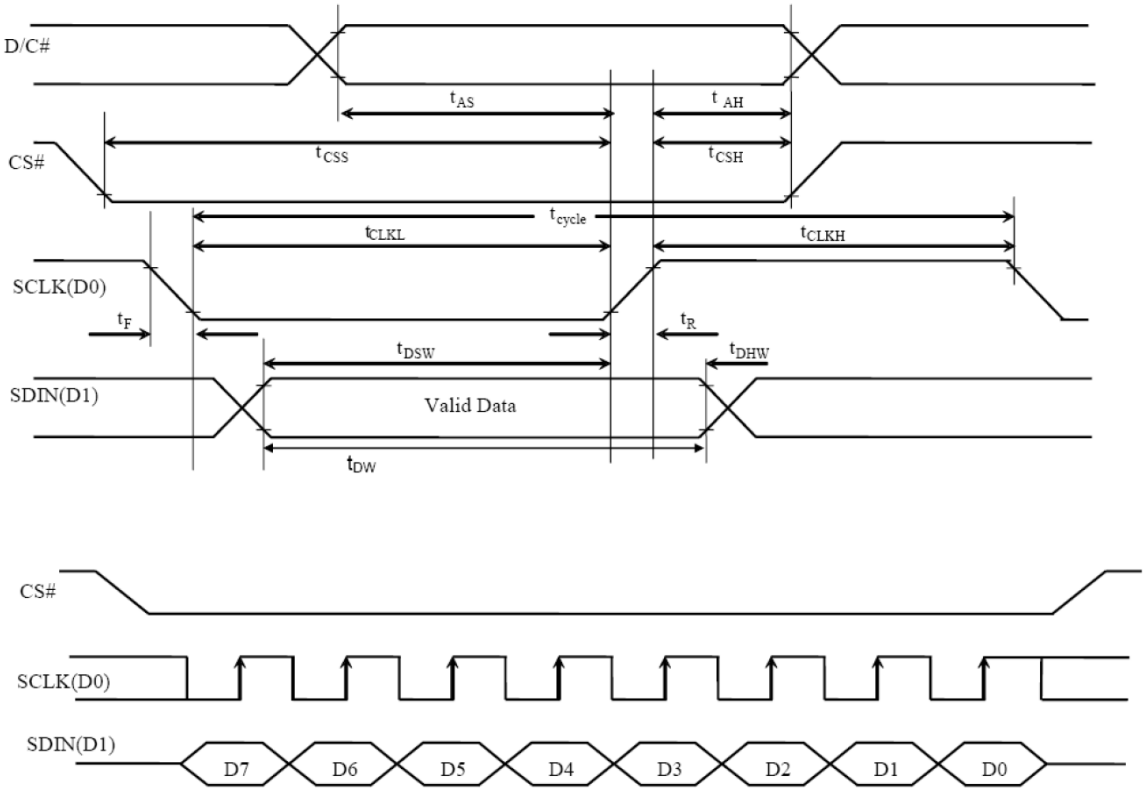


(*Write Timing*)

3.5.1.3 Serial Interface Timing Characteristics

V_{DD}-V_{SS} = 1.65V to 3.3V, Ta=25ºC

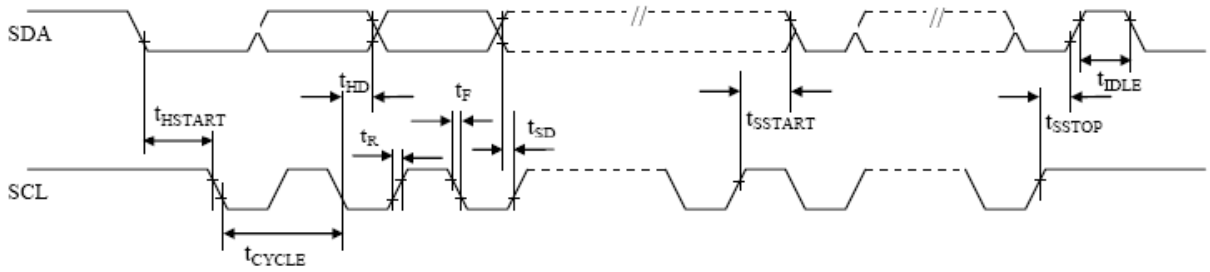
Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	50	-	ns
tDW	Data Write Time	55	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Serial Clock Low Time	100	-	ns
t_{CLKH}	Serial Clock High Time	100	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns



3.5.1.4 I²C Interface Timing Characteristics

V_{DD}-V_{SS} = 1.65V to 3.3V, Ta=25°C

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDAOUT" Pin) Data	0	-	ns
	Data Hold Time (for SDAin Pin)			
	Hold Time (for "SDAIN" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us



4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightnes	L_{br}	Note 5 on page 8	100	120	-	cd/m^2
C.I.E.(White)	(X)	C.I.E. 1931	0.25	0.29	0.33	-
	(Y)		0.27	0.31	0.35	
Dark Room Contrast	CR		-	>10,000:1	-	-
Viewing Angle				Free	-	degree

*Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12.5V.
Software configuration follows Section 5.4 Initialization

5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

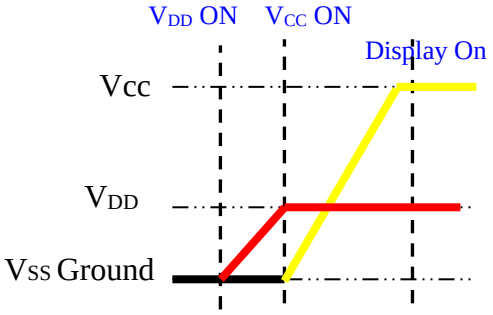
Please refer to the Technical Manual for the SSD1305

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

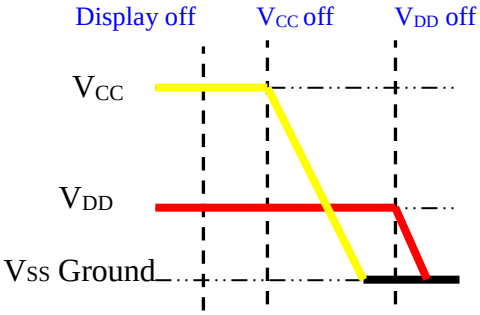
5.2.1 POWER UP SEQUENCE

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(when VDD is stable)
7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
(When V_{CC} reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 9:

1) Since an ESD protection circuit is connected between VDD, and VCC inside the driver IC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF.
2) VCC should be kept float (disable) when it is OFF.
3) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.
4) VDD should not be power down before VCC power down.

5.3 RESET CIRCUIT

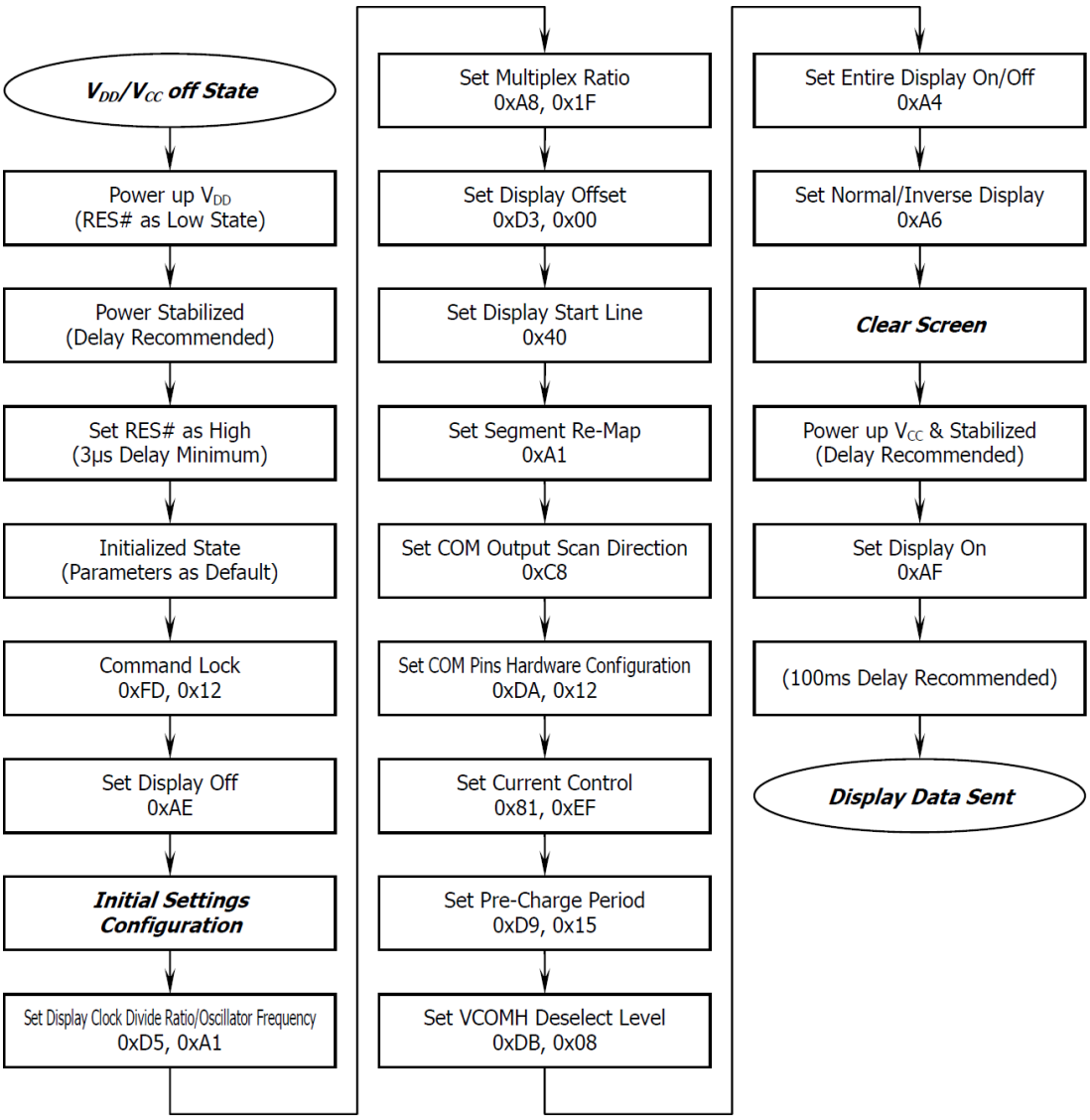
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128x64 Display mode
3. Normal segment and display data colume and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80h
9. Normal display mode (Equivalent to A4h command)

5.4 ACTUAL APPLICATION EXAMPLE

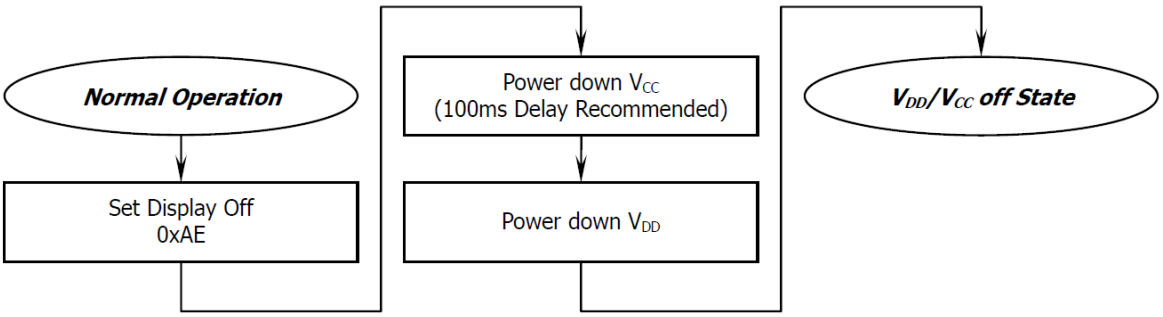
Command usage and explanation of an actual example

<Power up sequence>

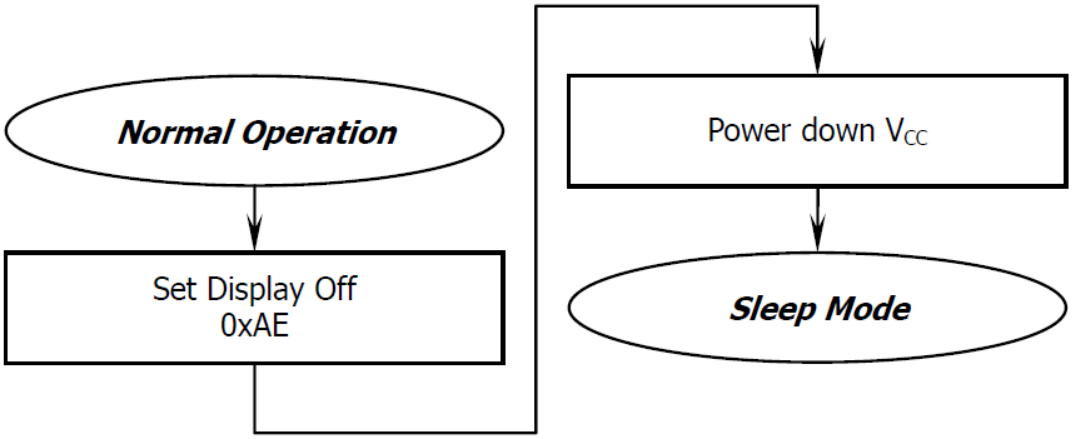


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

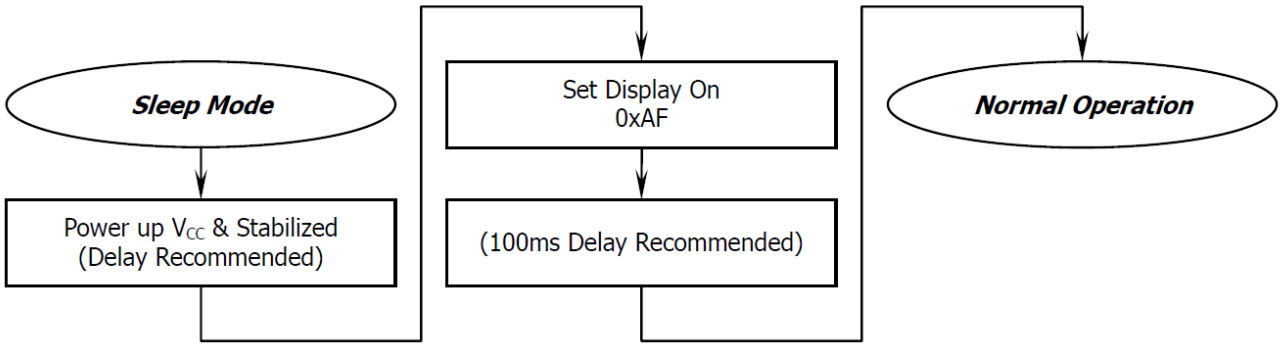
<Power down sequence>



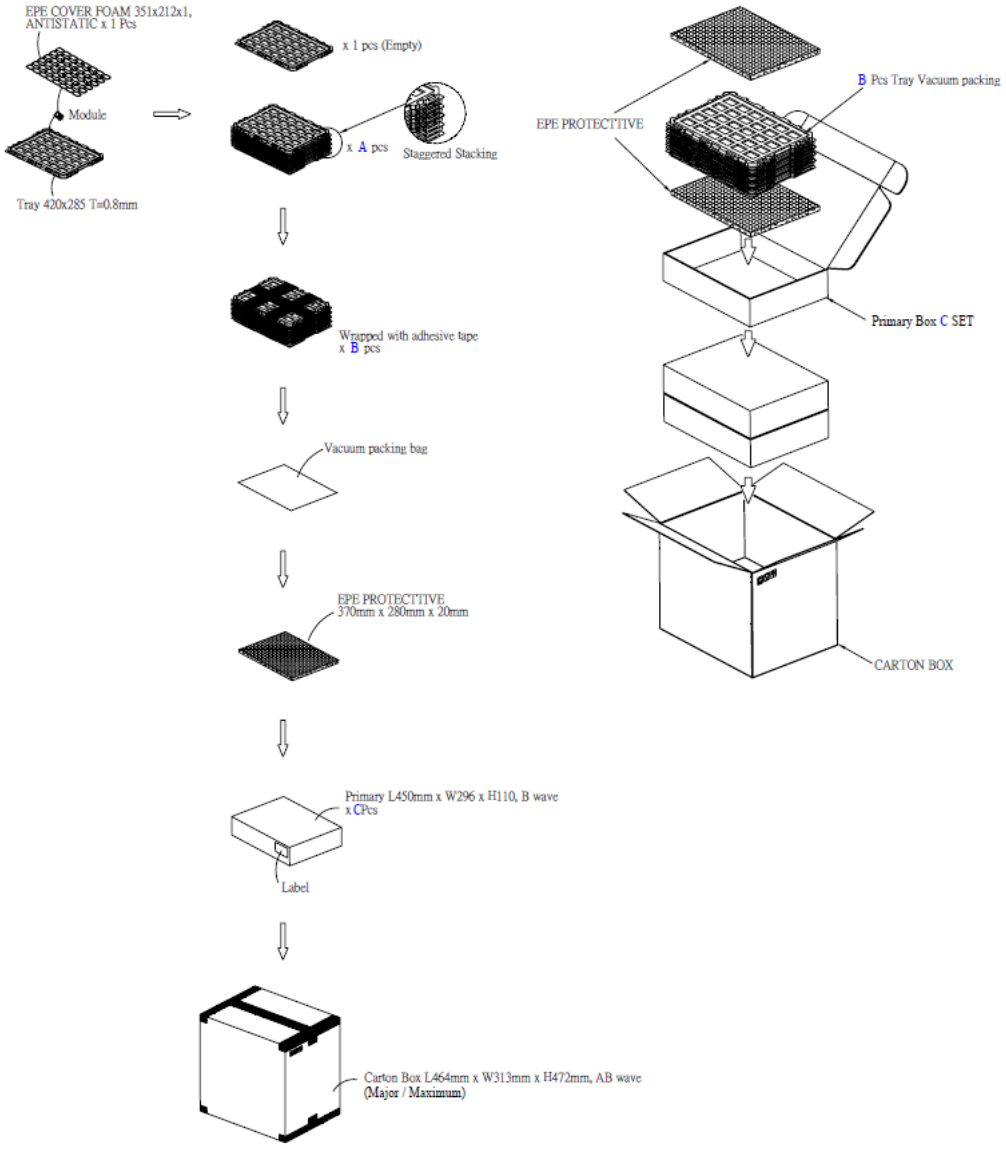
<Entering Sleep Mode>



<Exiting Sleep Mode>



6 PACKAGING AND LABELLING SPECIFICATION



Item		Quantity	
Holding Trays	(A)	15	per Primary Box
Total Trays	(B)	16	per Primary Box (Including 1 Empty Tray)
Primary Box	(C)	1~4	per Carton (4 as Major / Maximum)

6.1 LABELLING & MARKING

DENSITRON
DD-12832WE-1B
TW YY MM

7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

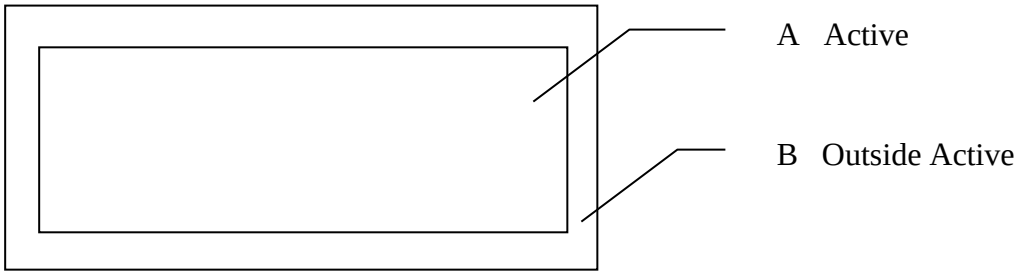
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assembly's standard

7.2.2 Zone definition



7.2.3 Environment Required

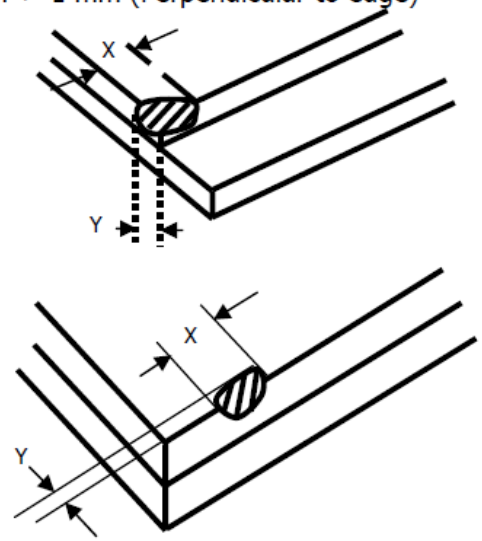
Test and measurement to be conducted under following conditions

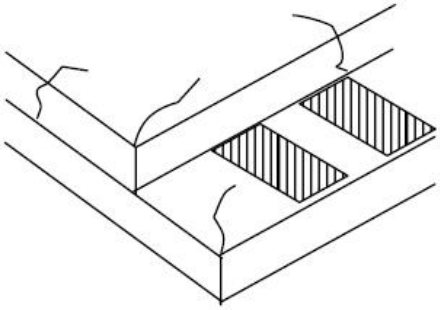
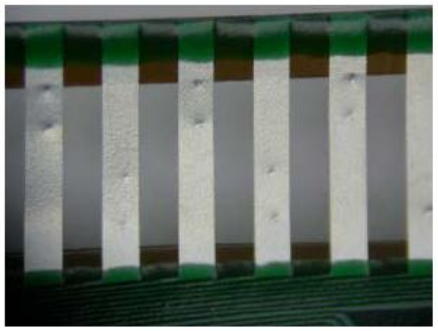
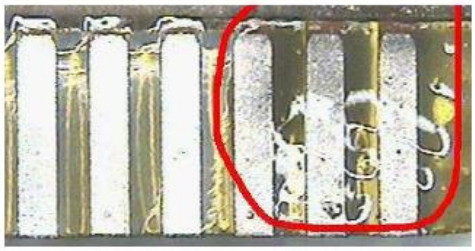
Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

7.2.4 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1	Defects in Cosmetic Check (Display Off)

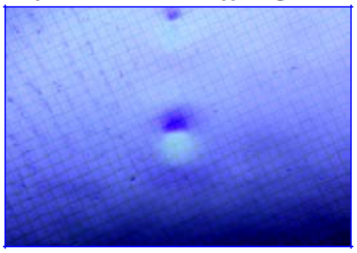
7.2.5 Cosmetic Check (Display Off) in Non Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

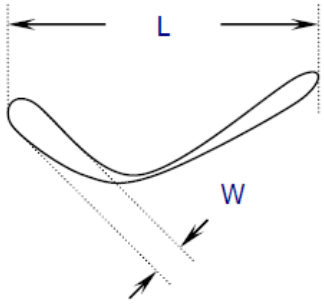
7.2.6 Cosmetic Check (Display Off) in Active Area

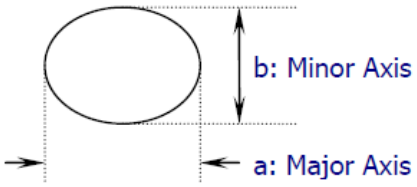
It is recommended to execute in clear room environment (class 10k) if actual in necessary

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

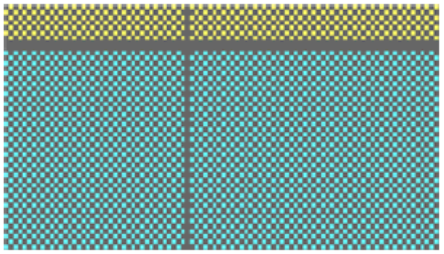
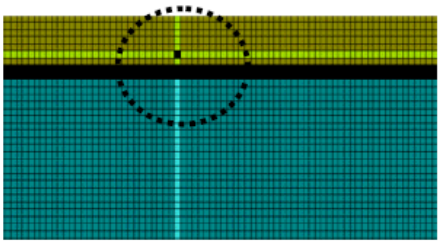
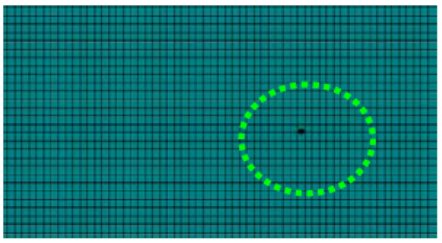
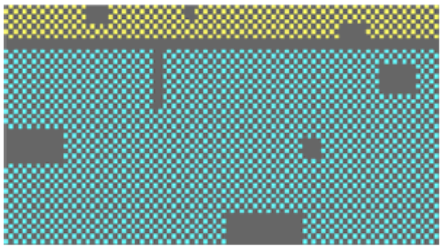
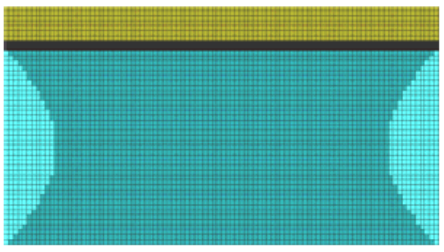
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2





7.2.7 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	85°C, 500 hours	No abnormalities in function and appearance
Low Temperature Operation	-40°C, 500 hours	No abnormalities in function and appearance
High Temperature Storage	90°C, 500 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C, 500 hours	No abnormalities in function and appearance
High Temperature/Humidity Operation	60°C, 90%RH, 240 hours	No abnormalities in function and appearance
Thermal Shock	100 cycles of -40°C ↔85°C 30 mins dwell	No abnormalities in function and appearance

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C; 55±15% RH

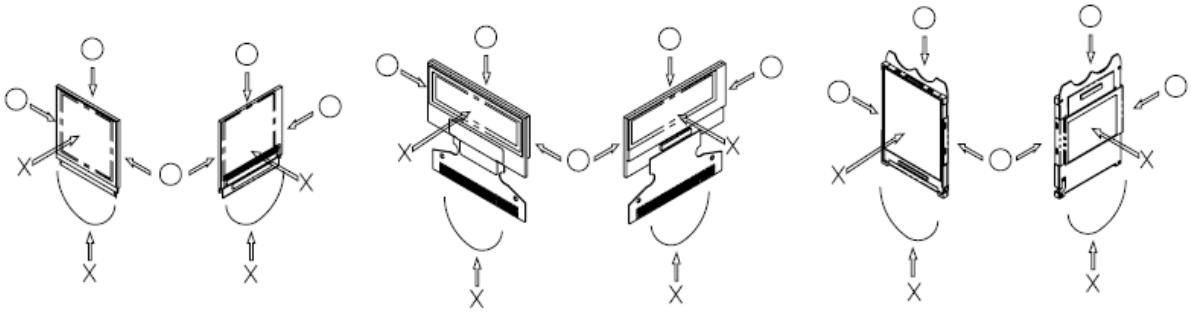
8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration for minimum: 10,000 hours under 120 cd/m² brightness 30,000 hours under 80 cd/m2 brightness 50,000 hours under 60 cd/m2 brightness and 50% Checkerboard, humidity (50% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.
2	Reduction in operating brightness will result in an extension of half-life obviously..

9 HANDLING PRECAUTIONS

9.1 HANDLING PRECAUTIONS

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

* Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 STORAGE PRECAUTIONS

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron Technologies Plc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 DESIGNING PRECAUTIONS

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066

* Connection (contact) to any other potential than the above may lead to rupture of the IC.

9.4 OTHER PRECAUTIONS

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

9.5 PRECAUTIONS WHEN DISPOSING OF THE OEL DISPLAY MODULES

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

10 SUPPORTED ACCESSORIES

10.1 DUO KIT

Densitron has developed an easy to use yet powerful development and demonstration tool for driving its range of Passive Matrix OLED displays from the USB port of a PC.
DUO (Densitron USB OLED) kit is hot pluggable and does not require extra cables or power supply to run, allowing users to be up and running in minutes.

The kit consists of an OLED display with transition Board, USB controller card, mini USB cable and a CD with software application and drivers.

Part number: PDK-N-12832WE-1B

10.2 TRANSITION BOARD CARD

A Transition board card is like a daughterboard which is meant to be a circuit board for connections between the baseboards (DUO).
It has connector pins for interfacing between the display and the baseboards.
It also includes the OLED display.
Part number: PDT-N-12832WE-1B

10.3 CONNECTOR BOARD CARD

A Connector board card is also a daughterboard which is a circuit board for connection between a microprocessor or microcontroller (customer's system).

Part number: EVK-CONNECT-015

10.4 CONNECTOR

Type: ZIF connector

No. of connections	Pitch (mm)	Manufacturer	Manufacturer part no.	Distributor part no.
24	0.50	Omron	XF2M-2415-1A	Farnell/1112559 Digikey/ OR721CT-ND