DMT026QVNXCSI-1A
PRODUCT SPECIFICATION

Version 0.1
Aug 10, 2023

TBD

Customer's Approval	
Signature	*Date*

Prepared by *Yvette Hsieh*
Approved by *Kenny Lin*

Revision History

VERSION	DATE	DESCRIPTION	AUTHOR
0.1	Aug 10, 2023	Preliminary	Yvette Hsieh

Legal Notice

Table of Contents

1. General Description

1.1 Introduction

This is a 2.6” size colour active matrix TFT LCD module that uses amorphous silicon TFT as a switching device. The display is normally black mode, transmissive, and featuring high contrast and excellent colour saturation. The resolution of the TFT-LCD is 240 x 320 and can display up to 262K colours. The display module supports 8/9/16/18-bit MCU interface, 3/4 SPI + 16/18-bit RGB interface, 3-/4-line serial interface, and tape bonding touch panel.

1.2 Main Features

Item	Contents
Display Type	TFT LCD
Screen Size	2.6” Diagonal
Display Format	240 x RGB x 320 Dots
No. of Colour	65K/262K
Overall Dimensions	46.00 (W) x 64.00 (H) x 4.08 (D) mm
Active Area	39.6 (W) x 52.8 (H) mm
Mode	Normally Black / Transmissive
Surface Treatment	Glare (6H)
Viewing Direction	All round
Interface	8/9/16/18-bit MCU, 3/4 SPI + 16/18-bit RGB, 3-/4-line serial
Driver IC	ST7789V
Backlight Type	LED, Whites, 6 chips
Touch Panel	PCT
Touch Interface	I^2C
Bonding Type	Tape Bonding
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
ROHS	Compliant to RoHS 2.0

1.3 Touch Features

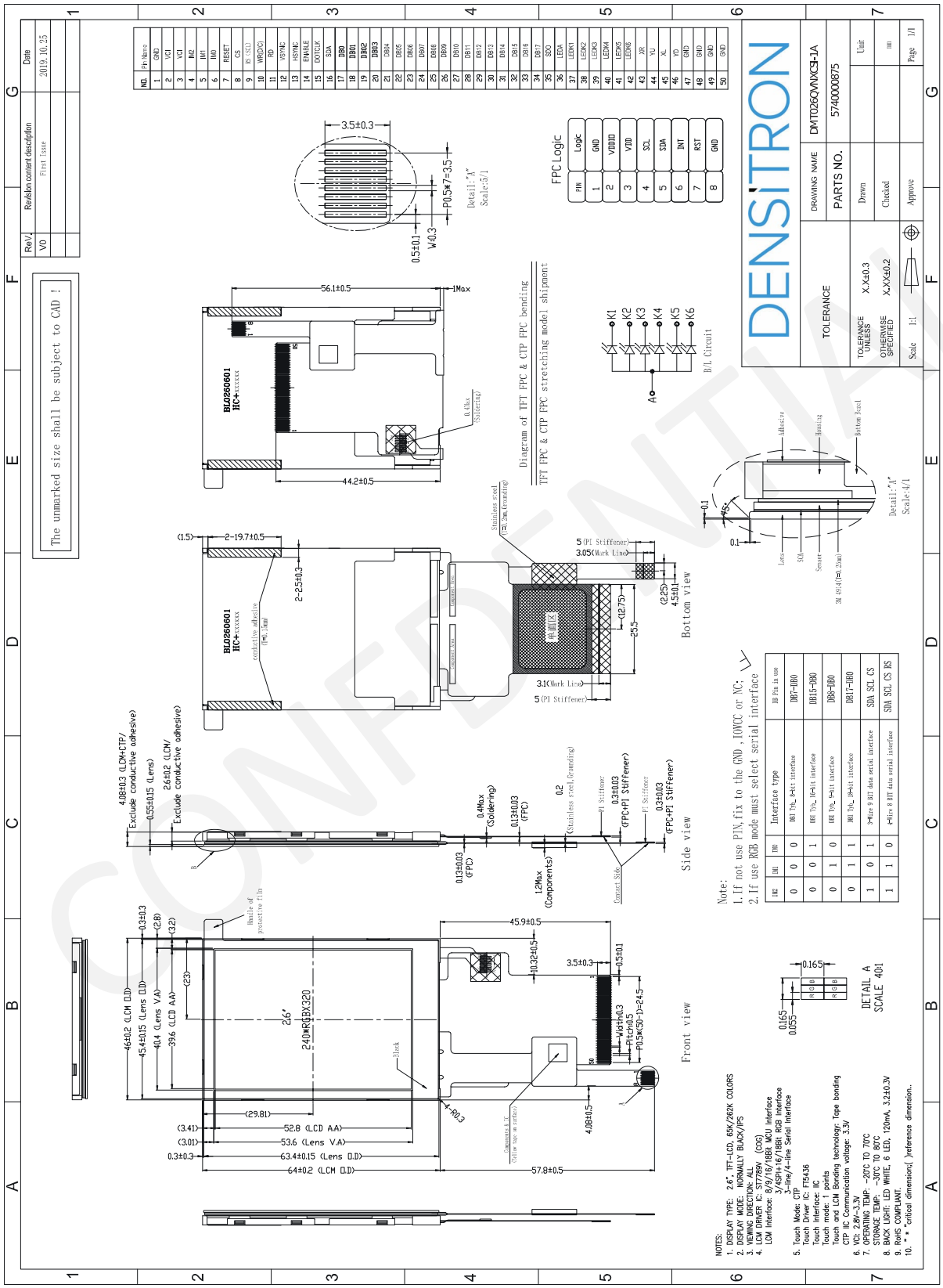
Item	Contents
Structure	G+G
Controller IC	FT5436
Interface	I^2C
Slave Address	0x38(7bit)/8bit:0x70(Write) 0x71(Read)
Touch mode	Single point and Gestures
Logic Level	3.3V

2. Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Display Format	240 x RGB x 320	Dots
Overall Dimensions	46.00 (W) x 64.00 (H) x 4.08 (D)	mm
Active Area	39.6 (W) x 52.8 (H)	mm
Dot Pitch	0.165 (W) x 0.165 (H)	mm
Weight	20	g
IC Controller/Driver	ST7789V	

2.2 Mechanical Drawing



3. Electrical Specification

3.1 Absolute Maximum Ratings

(Ta=25°C, VSS=0V)

Item	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Operating Temperature	T_{OP}	-20	+70	°C
Storage Temperature	T_{ST}	-30	+80	°C

Note 1: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. For normal operations, it is desirable to use this module under the conditions according to Section 3.2 “Electrical Characteristics”, to avoid malfunctioning.

Note 2: Please refer to item of RELIABILITY.

3.2 Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit
Digital Supply Voltage	VCI	2.4	3.3	3.6	V
Normal Mode Current Consumption	IDD	-	6	12	mA
Level Input Voltage	V_{IH}	0.7 VCI	-	VCI	V
	V_{IL}	GND	-	0.3 VCI	
Level Output Voltage	V_{OH}	0.8 VCI	-	VCI	V
	V_{OL}	GND	-	0.2 VCI	

3.3 Interface Pin Assignment

3.3.1 TFT Pin Define

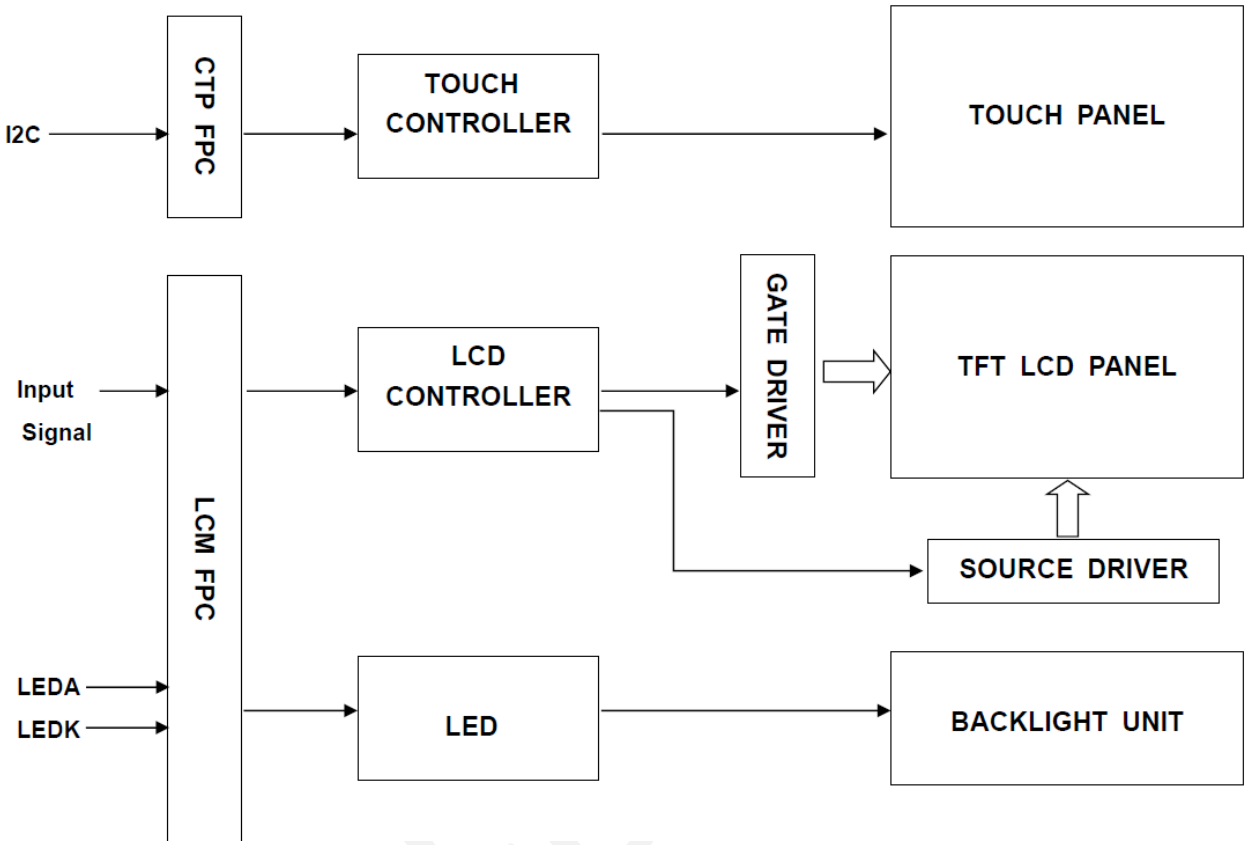
<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>GND</td><td>P</td><td>Ground.</td></tr>
<tr><td>2-3</td><td>VCI</td><td>P</td><td>Power supply voltage (3.3 V)</td></tr>
<tr><td>4</td><td>IM2</td><td>I</td><td rowspan="3">Interface Selecting signal
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface Type</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Tyb_ 18-bit interface</td><td>DB17-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Tyb_16-bit interface</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Tyb_9-bit interface</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Tyb_18-bit interface</td><td>DB17-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface</td><td>SDA SCL CS</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface</td><td>SDA SCL CS RS</td></tr>
</table></td></tr>
<tr><td>5</td><td>IM1</td><td>I</td></tr>
<tr><td>6</td><td>IM0</td><td>I</td></tr>
<tr><td>7</td><td>REST</td><td>I</td><td>This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active.</td></tr>
<tr><td>8</td><td>CS</td><td>I</td><td>System bus select signal.
Low: Select (accessible). High: Not select (inaccessible)</td></tr>
<tr><td>9</td><td>RS (SPI-SCL)</td><td>I</td><td>(D/CX): This pin is used to select “Data or Command” in the parallel interface. When DCX = 1, data is selected. When DCX = 0, command is selected. (SCL): This pin is used as the serial interface clock in 3wire 9bit/4wire 8bit serial data interface. If not used, this pin should be connected to VCI</td></tr>
<tr><td>10</td><td>WR (SPI—RS)</td><td>I</td><td>(WRX) 8080/8080 Ⅰ Ⅱ system: Serves as a write signal and writes data at the rising edge.
(D/CX) 4line system: Serves as the select or of command or parameter. Fix to VCI level when not in use.</td></tr>
<tr><td>11</td><td>RD</td><td>I</td><td>Read strobe signal. Data are read when RDX is low. If not used, please connect this pin to VCI.</td></tr>
<tr><td>12</td><td>VSYNC</td><td>I</td><td>Frame synchronous signal. Low active. Connect to I GND when DPI is not selected.</td></tr>
<tr><td>13</td><td>HSYNC</td><td>I</td><td>Line synchronous signal. Low active</td></tr>
<tr><td>14</td><td>ENABLE</td><td>I</td><td>Data enable signal in DPI operation.
Low: Select (Accessible). High: Not select (Inaccessible)
Connect to GND when DPI is not selected.</td></tr>
<tr><td>15</td><td>DOTCLK</td><td>I</td><td>Pixel clock signal. The data input timing is set on the rising edge. Connect to GND when DPI is not selected.</td></tr>
</table>

No.	Symbol	I/O	Function
16	SDA	I	Pixel clock signal. The data input timing is set on the rising edge. Connect to GND when DPI is not selected.
17-34	DB0-DB17	I/O	Data bus. In 16 Bit RGB Interface mode, use DB1-DB11, DB13-DB17. In 18 Bit RGB Interface mode, use DB0-DB17. Connect to GND when is not used.
35	SDO	O	This pin is enabled when SDOE=1 and DBI Type C is used. With this setting, SDA can be used as an input pin and SDO pin can be used as an output pin without bidirectional bus to exe cute serial communication. If not used, please open.
36	LEDA	P	Anode pin of backlight
37-42	LEDK1-KEDK6	P	Cathode pin of backlight
43	XR (NC)	-	Touch panel right glass terminal
44	YU (NC)	-	Touch panel top film terminal
45	XL (NC)	-	Touch panel left glass terminal
46	YD (NC)	-	Touch panel bottom film terminal
47-50	GND	P	Ground

3.3.2 CTP Pin Define

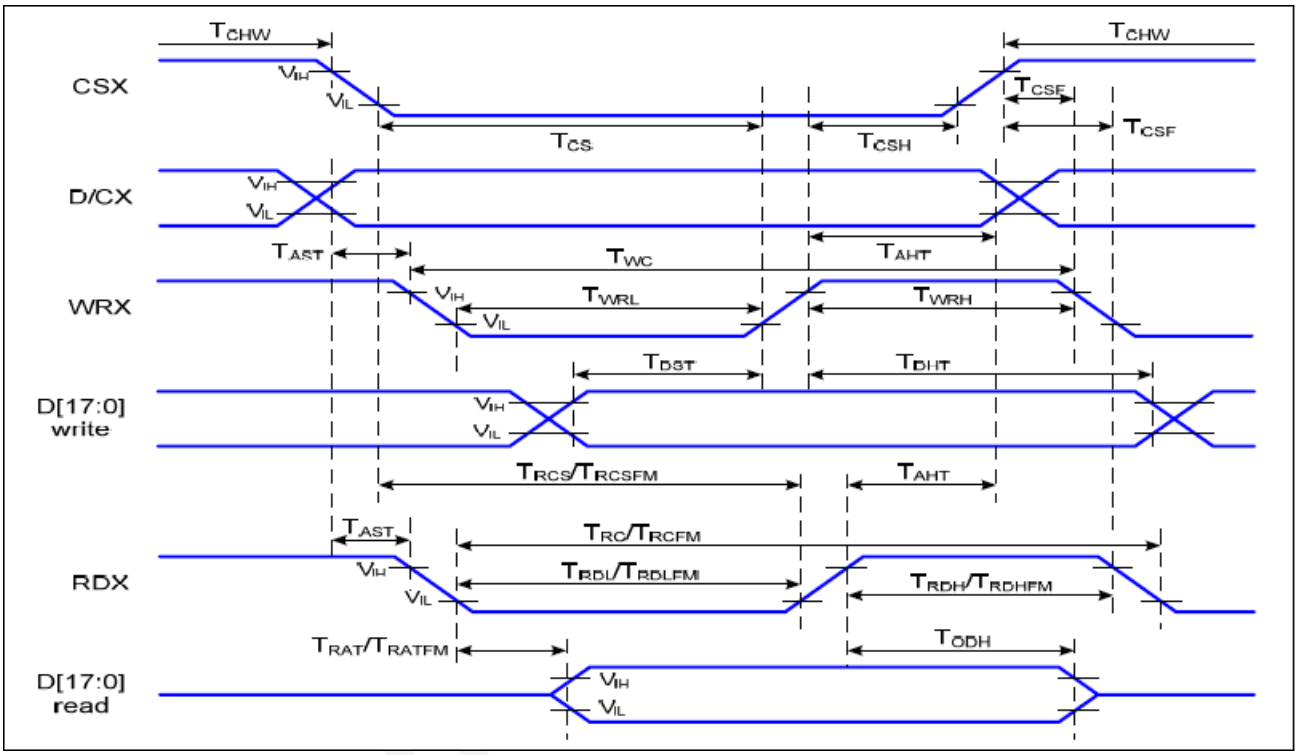
NO.	Symbol	I/O	Function
1	GND	P	Ground.
2	VDDIO	P	I/O power supply voltage.
3	VDD	P	Supply voltage.
4	SCL	I	I^2C clock input.
5	SDA	I/O	I^2C data input and output
6	INT	I	External interrupt to the host.
7	RST	I	External Reset, Low is active.
8	GND	P	Ground.

3.4 Block Diagram



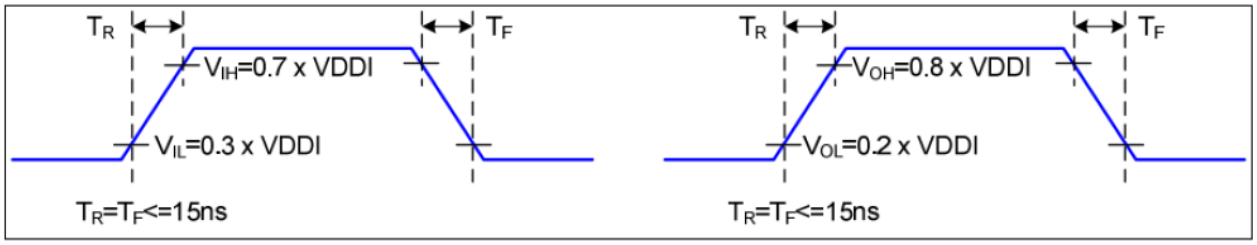
3.5 Timing Characteristics

3.5.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

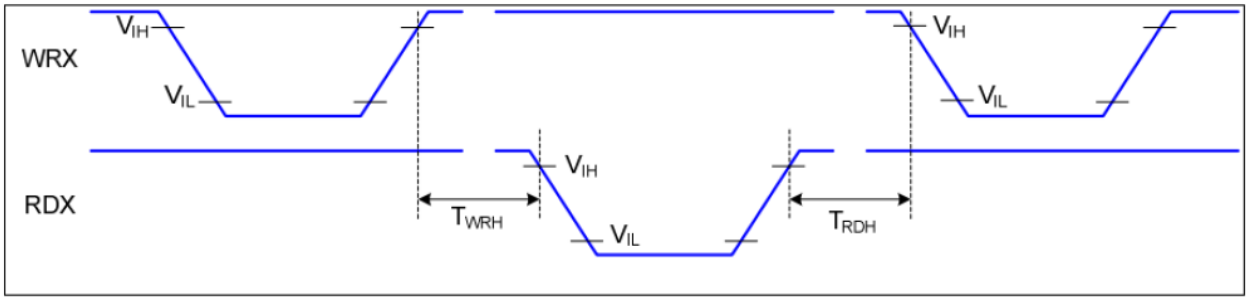


Signal	Symbol	Parameter	Min	Max	Unit	Conditions
DCX	T_{AST}	Address setup time	0	-	ns	-
	T_{AHT}	Address hold time (Write/Read)	10	-	ns	-
CSX	T_{CHW}	Chip select H pulse width	0	-	ns	-
	T_{CS}	Chip select setup time (Write)	15	-	ns	-
	T_{RCS}	Chip select setup time (Read ID)	45	-	ns	-
	T_{RCSFM}	Chip select setup time (Read FM)	355	-	ns	-
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	-
	T_{CSH}	Chip select hold time	10	-	ns	
WRX	T_{WC}	Write cycle	66	-	ns	-
	T_{WRH}	Control pulse H duration	15	-	ns	-
	T_{WRL}	Control pulse L duration	15	-	ns	-
RDX (FM)	T_{RCFM}	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	T_{RDHFM}	Control H duration (FM)	90	-	ns	
	T_{RDLFM}	Control L duration (FM)	355	-	ns	
RDX (ID)	T_{RC}	Read Cycle (ID)	160	-	ns	When read ID data
	T_{RDH}	Control pulse H duration (ID)	90	-	ns	
	T_{RDL}	Control pulse L duration (ID)	45	-	ns	
DB [17:0]	T_{DST}	Data setup time	10	-	ns	For CL = 30pF
	T_{DHT}	Data hold time	10	-	ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Rising and falling timing for I/O signal

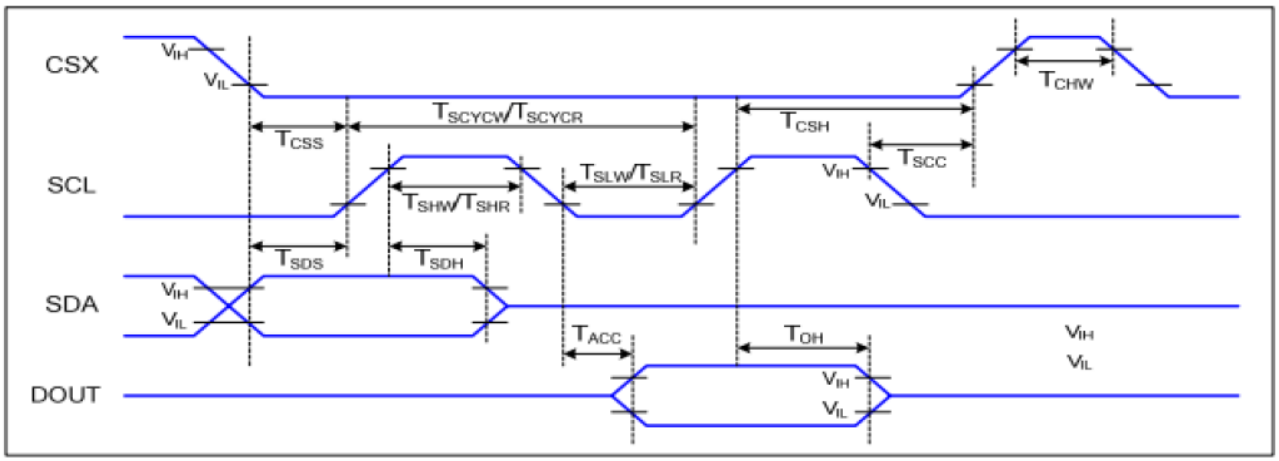


Write to Read and Read to Write timing



Note: The rising time and falling time (Tr, Tf) of input signal and fall time area specified at 15ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

3.5.2 Serial Interface Characteristics (3-line serial)

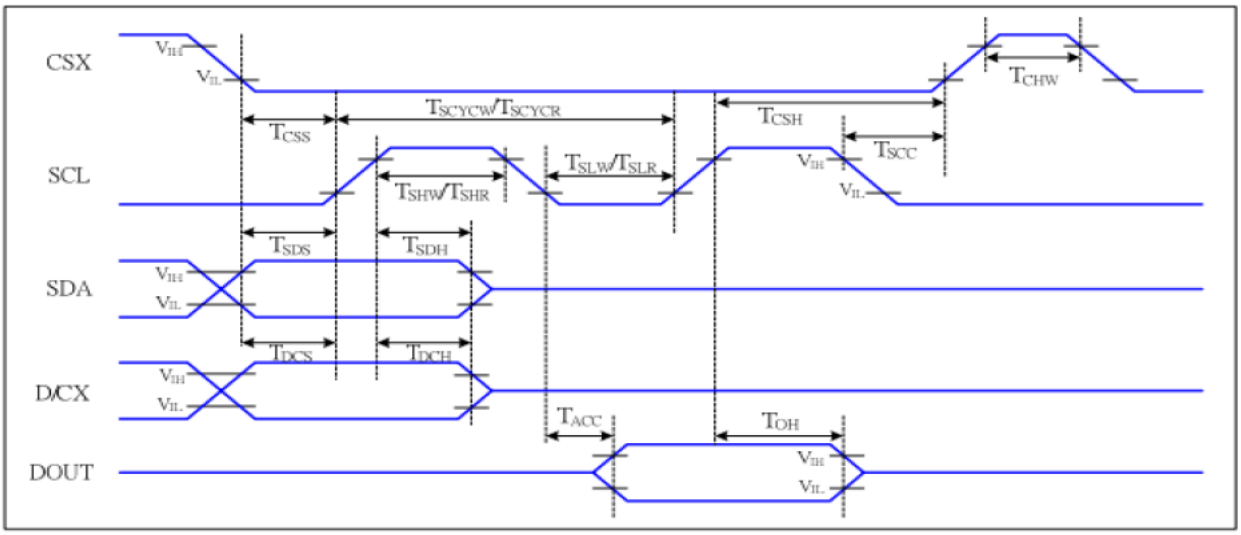


(VDDI=16.5 to 3.3V, VDD=2.4 to 3.3Vm AGND=DGND=0V, Ta=25°C)

Signal	Symbol	Parameter	Min	Max	Unit	Conditions
CSX	T_{CSS}	Chip select setup time (write)	15	-	ns	-
	T_{CSH}	Chip select hold time (write)	15	-	ns	-
	T_{CSS}	Chip select setup Time (read)	60	-	ns	-
	T_{SCC}	Chip select hold time (read)	65	-	ns	-
	T_{CHW}	Chip select H pulse width	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (wite)	66	-	ns	-
	T_{SHW}	SCL H pulse width (wite)	15	-	ns	-
	T_{SLW}	SCL L pulse width (wite)	15	-	ns	-
	T_{SCYCR}	Serial clock cycle (rad)	150	-	ns	-
	T_{SHR}	SCL H pulse width (read)	60	-	ns	-
	T_{SLR}	SCL L pulse width (read)	60	-	ns	-
SDA (DIN)	T_{SDS}	Data setup time	10	-	ns	-
	T_{SDH}	Data hold time	10	-	ns	-
DOUT	T_{ACC}	Access time	10	50	ns	For maximum, CL=30pF. For minimum, CL=8Pf.
	T_{OH}	Output disable time	15	50	ns	

Note: The rising time and falling time (Tr, Tf) of input signal and fall time area specified at 15ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

3.5.3 Serial Interface Characteristics (4-line serial)



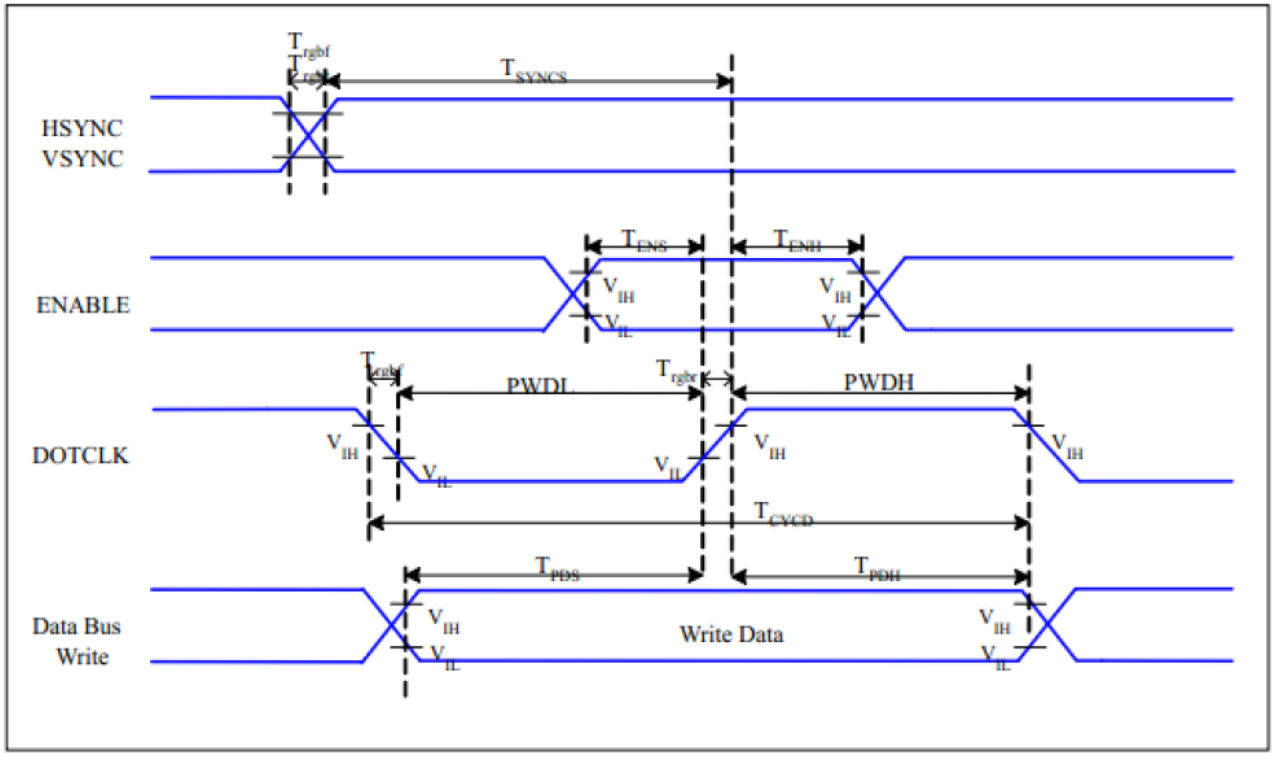
(VDDI=16.5 to 3.3V, VDD=2.4 to 3.3Vm AGND=DGND=0V, Ta=25°C)

Signal	Symbol	Parameter	Min	Max	Unit	Conditions
CSX	T_{CSS}	Chip select setup time (write)	15	-	ns	-
	T_{CSH}	Chip select hold time (write)	15	-	ns	-
	T_{CSS}	Chip select setup Time (read)	60	-	ns	-
	T_{SCC}	Chip select hold time (read)	65	-	ns	-
	T_{CHW}	Chip select H pulse width	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (wite)	66	-	ns	write command and data ram
	T_{SHW}	SCL H pulse width (wite)	15	-	ns	
	T_{SLW}	SCL L pulse width (wite)	15	-	ns	
	T_{SCYCR}	Serial clock cycle (rad)	150	-	ns	read command and data ram
	T_{SHR}	SCL H pulse width (read)	60	-	ns	
	T_{SLR}	SCL L pulse width (read)	60	-	ns	
D/CX	T_{DCS}	D/CX setup time	10	-	ns	-
	T_{DCH}	D/CX hold time	10	-	ns	-
SDA (DIN)	T_{SDS}	Data setup time	10	-	ns	-
	T_{SDH}	Data hold time	10	-	ns	-

DOUT	T_{ACC}	Access time	10	50	ns	For maximum, CL=30pF. For minimum, CL=8Pf.
	T_{OH}	Output disable time	15	50	ns	

Note: The rising time and falling time (Tr, Tf) of input signal and fall time area specified at 15ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

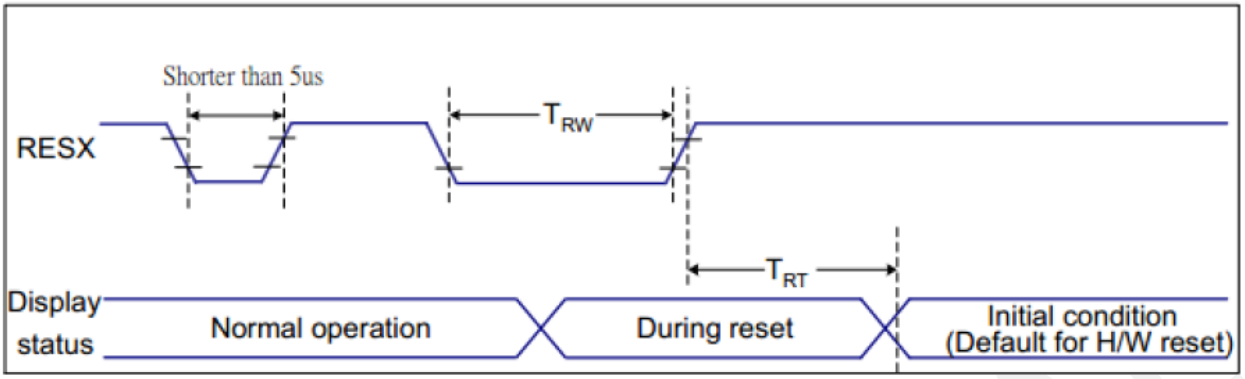
3.5.4 RGB Interface Characteristics



(VDDI=16.5 to 3.3V, VDD=2.4 to 3.3Vm AGND=DGND=0V, Ta=25˚C)

Signal	Symbol	Parameter	Min	Max	Unit
VSYNC/ HSYNC	TSYNCS	VSYNC/HSYNC setup time	30	-	ns
ENABLE	TENS	ENABLE setup time	25	-	ns
	TENH	ENABLE hold time	25	-	ns
DB	TPDS	PD Data setup time	50	-	ns
	TPDH	PD Data hold time	50	-	ns
DOTCLK	PWDH	DOTCLK high-level pulse width	60	-	ns
	PWDL	DOTCLK low-level pulse width	60	-	ns
	TCYCD	DOTCLK cycle time	120	-	ns
	Trghr, Trghf	DOTCLK rise/fall time	-	20	ns

3.5.5 Reset Timing Characteristics



Reset Timing

(VDDI=16.5 to 3.3V, VDD=2.4 to 3.3Vm AGND=DGND=0V, Ta=25˚C)

Related Pins	Symbol	Parameter	Min	Max	Unit	Note
RESX	TRW	Reset pulse width	10	-	us	-
	TRT	Reset cancel	-	5	ms	1, 5
				120	ms	1, 6, 7

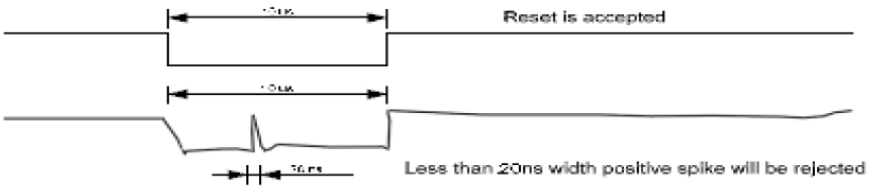
Note 1: The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).

Note 2: Spike due to and electrostatic discharge on RESX line does not caused irregular system reset according to the table bel

RESX Pulse	Action
Shorter than 5us	Reset rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

Note 3: During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode) and then return to the default condition for the Hardware Reset.

Note 4: Spike Rejection can also be applied during a valid reset pulse, as shown below:



Note 5: When Reset applied during Sleep In mode

Note 6: When Reset applied during Sleep Out mode

It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

4. Electrical Specification Touch

4.1 Electrical Characteristics

4.1.1 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Power Supply Voltage	VDD	2.7	3.6	V
I/O Digital Voltage	VDDIO	1.8	3.6	V

4.1.2 DC Electrical Characteristics

(Ta=25°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	2.7	3.3	3.47	V	-
I/O Digital Supply Voltage	VDDIO	1.8	-	3.6	V	-
Normal Mode Operating Current	-	-	11	-	mA	-
Sleep Mode Operating Current	-	-	42	-	μA	-
Monitor Mode Operating Current	-	-	0.43	-	mA	-
Digital Input Low Voltage	VIL	-0.3	-	0.3 VDDIO	V	-
Digital Input High Voltage	VIH	0.7 VDDIO	-	VDDIO	V	-
Digital Output Low Voltage	VOL	-	-	0.3 VDDIO	V	-
Digital Output Hogh Voltage	VOH	0.7 VDDIO	-	-	V	-

4.2 AC Electrical Characteristics

AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min	Typ.	Max
OSC clock 1	fosc1	VDD3= 2.8V, Ta=25°C	49	50	51

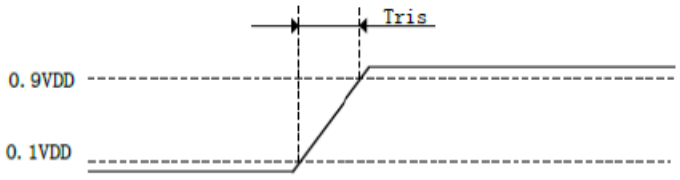
AC Characteristics of TX & RX

Item	Symbol	Min	Typ.	Max	Unit
TX Acceptable Clock	ftx	50	150	400	KHz
TX Output Rise Time	Ttxr	-	210	-	ns
TX Output Fall Time	Ttxf	-	210	-	ns
RX Input Voltage	Trxi	1.2	-	1.6	V

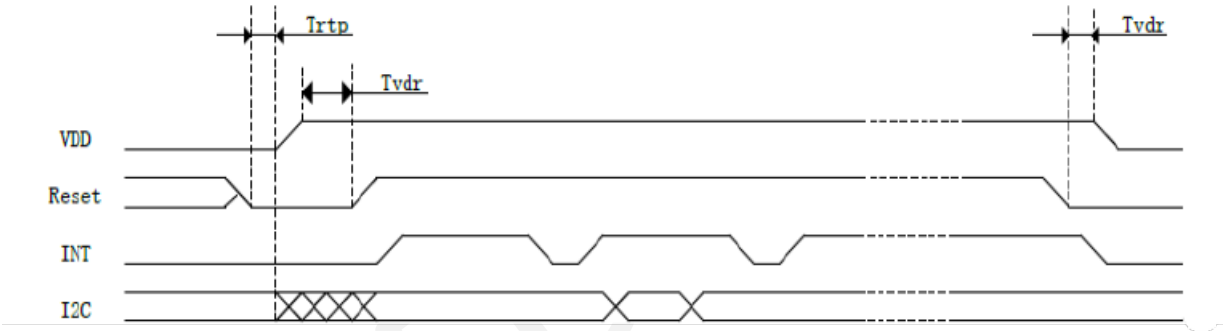
4.3 Power ON/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I^2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

Power on time

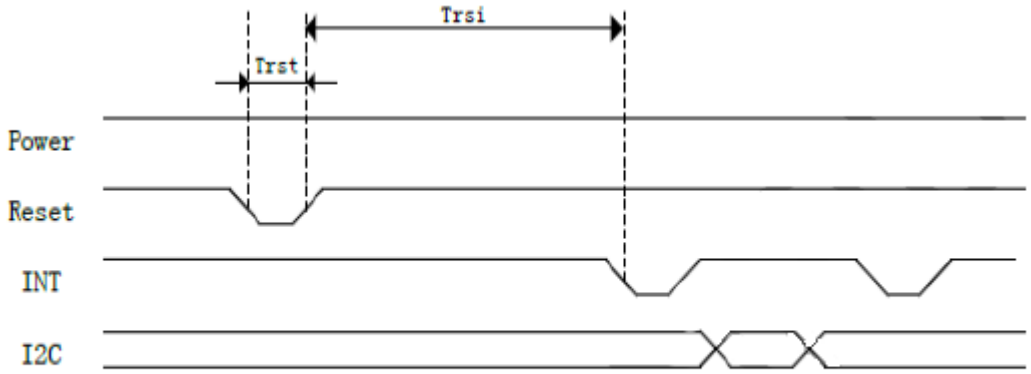


Power cycle requirement



Power on sequence

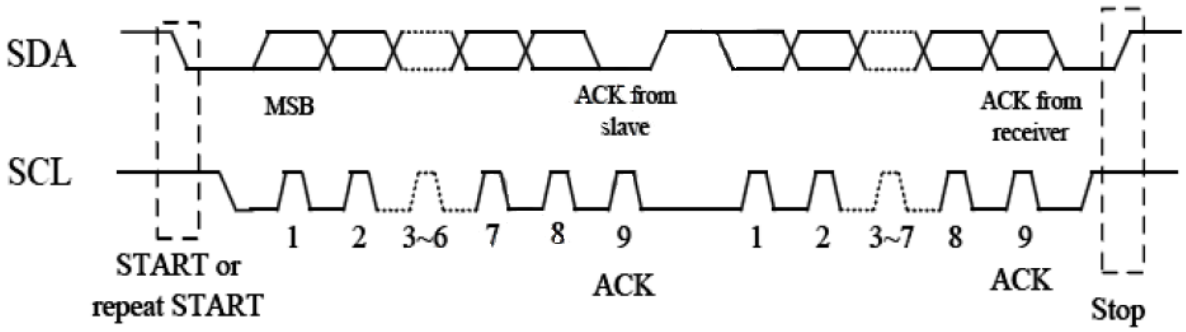
Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on



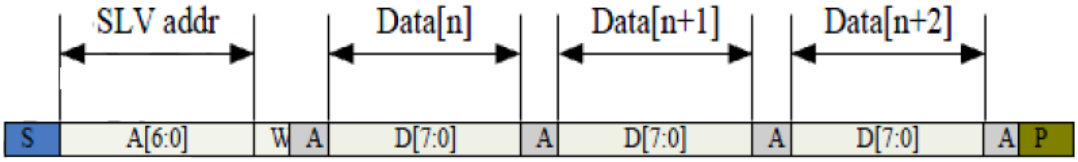
Parameter	Description	Min	Max	Unit
Tris	Rise time from 0.1VDD to 0.9VDD	-	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	-	ms
Trtp	Time of resetting to be low before powering on	100	-	us
Tvdr	Reset time after VDD powering on	1	-	ms
Trsi	Time of starting to report point after resettng	-	200	ms
Trst	Reset time	1	-	ms

4.4 I²C Timing

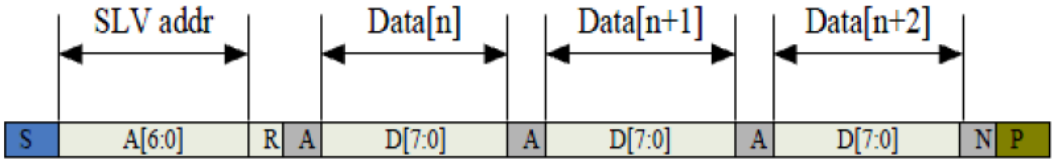
FT5436 support the I²C interface, which can be used by a host processor or the devices. The I²C is always configured in the Slave mode. The data transfer format is shown below.



I²C master write, slave read



I²C master read, slave write



Mnemonics	Description
S	I²C start on I²C reset
A [6:0]	Slave address
R/W	Read/Write bit, “1” for read, “0” for write
A (N)	ACK (NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet

I²C interface Timing

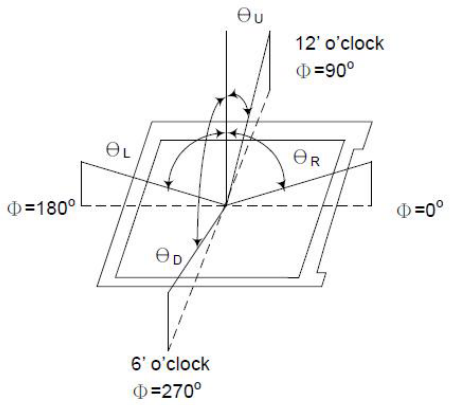
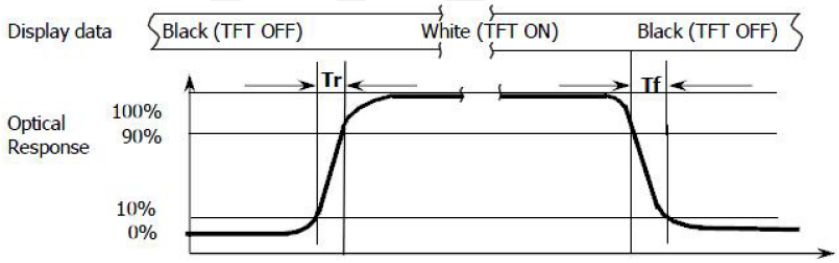
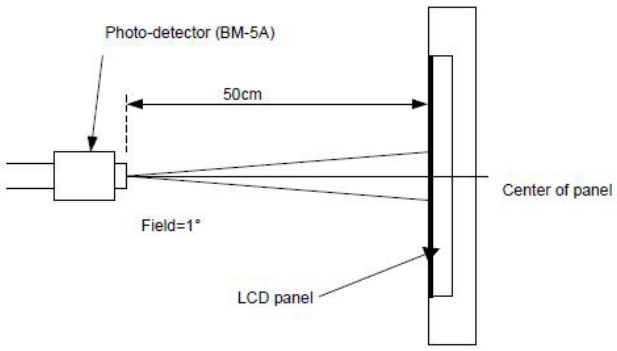
Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3	-	us
Hold Time (repeated) START condition	0.6	-	us
Data setup time	100	-	ns
Setup time for a repeated START condition	0.6	-	us
Setup time for STOP condition	0.6	-	us

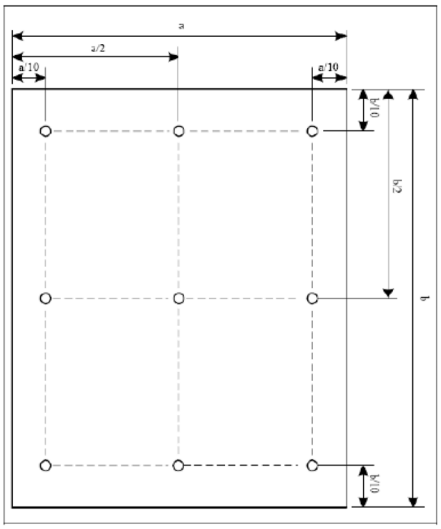
5. Optical Specification

5.1 Optical Characteristics

Characteristics		Symbol	Conditions	Min	Typ	Max	Unit	Note
Contrast Ratio		CR	θ = 0° Normal viewing angle	400	500	-	-	1, 2
Response time		$T_R + T_F$		-	35	50	msec	1, 3
Color Gamut		S (%)	-	58	58	-	%	-
Viewing Angle	Left	ΘL	CR>10	60	80	-	deg	1, 4
	Right	ΘR		60	80	-		
	Up	ΘU		60	80	-		
	Down	ΘD		60	80	-		
Colour Chromaticity	Red	Rx	θ = 0° Normal viewing angle	0.580	0.620	0.660	-	1, 4 CA-310
		Ry		0.325	0.365	0.405		
	Green	Gx		0.293	0.333	0.373		
		Gy		0.549	0.589	0.629		
	Blue	Bx		0.117	0.157	0.197		
		By		0.045	0.085	0.125		
	White	Wx		0.255	0.295	0.335		
		Wy		0.283	0.323	0.363		
Luminance		Lv	-	350	400	-	cd/m^2	5
Uniformity		Avg	-	80	-	-	%	5

Note: Measuring Condition = in dark room, at ambient temperature 25±2℃, for 15 min warm-up time.

Note	Item	Test method
1	Definition of Viewing Angle	
2	Definition of Contrast Ratio (CR)	$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$
3	Definition of Response Time	
4	Definition of Optical Measurement Setup	

Note	Item	Test method
5	Definition of Luminance Uniformity	 $\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$ $\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$

6. LED Backlight Specification

6.1 LED Backlight Characteristics

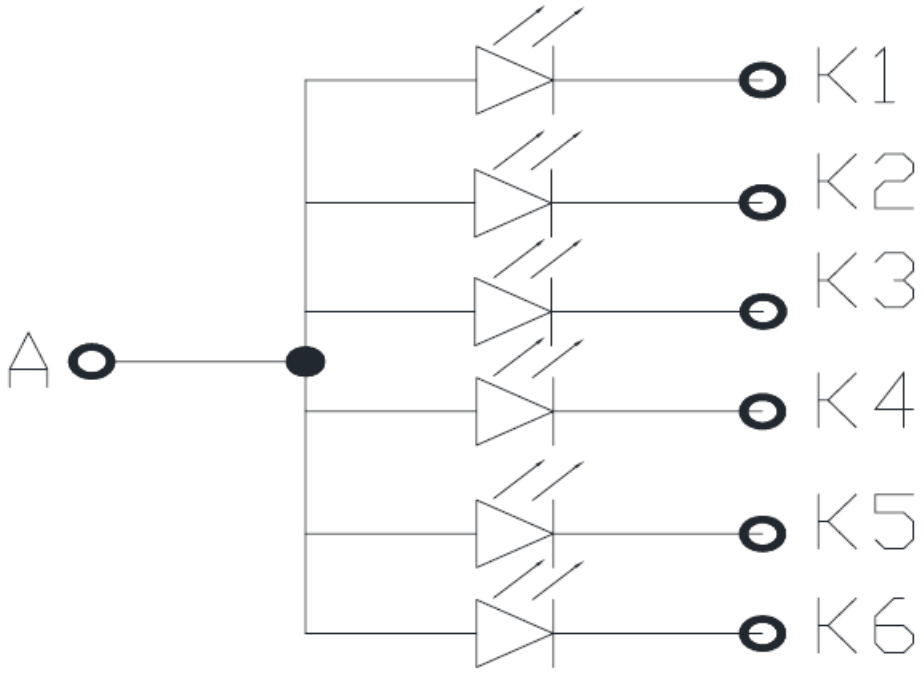
The back-light system is edge-lighting type with 6 chips White LED

Item	Symbol	Min	Typ	Max	Unit	Note
Forward Current	I_F	90	120	-	mA	-
Forward Voltage	V_F	-	3.2	-	V	-
LED Lifetime	Hr	50000	-	-	Hour	1, 2

Note 1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

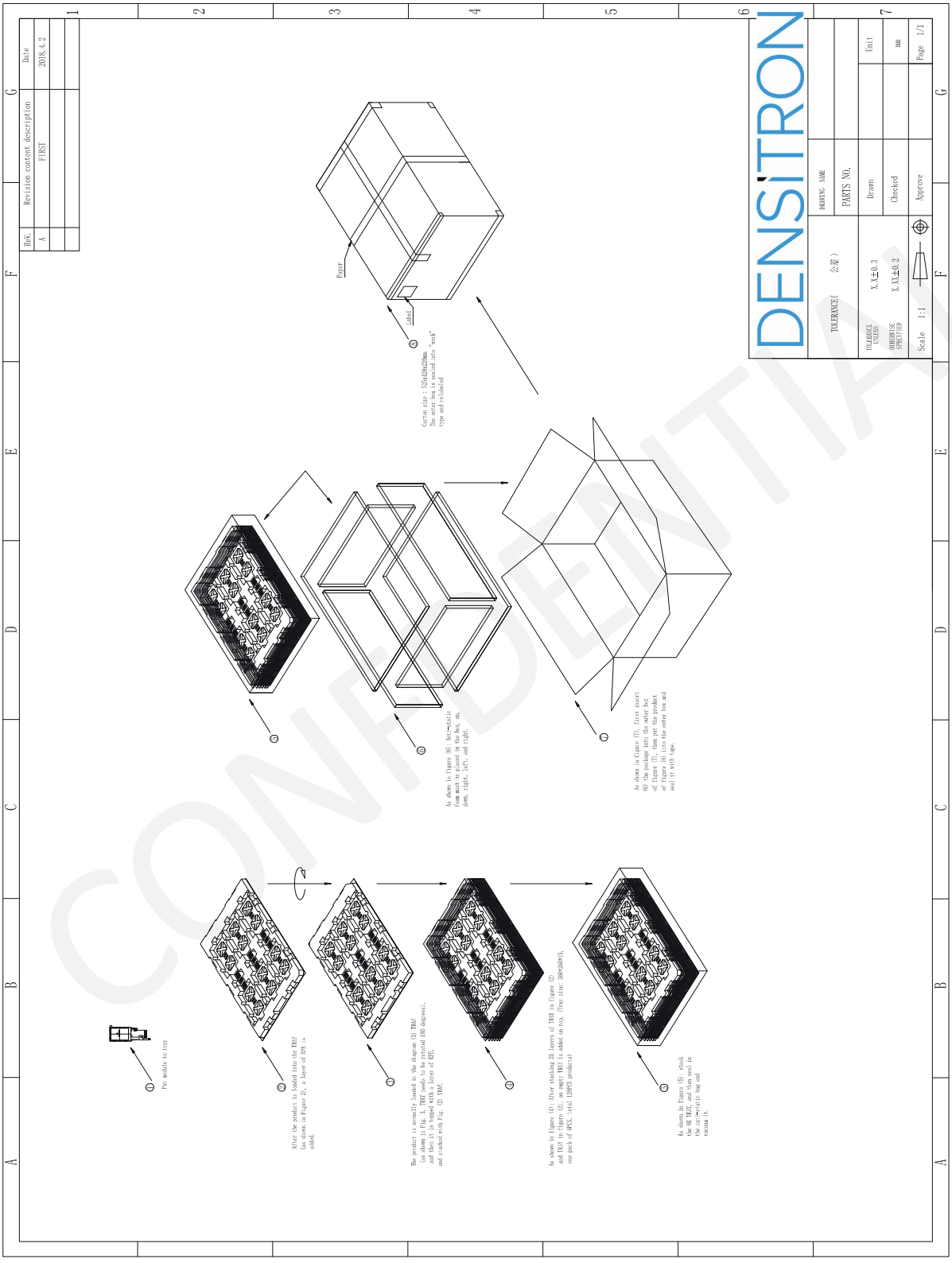
Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=120mA. The LED lifetime could be decreased if operating IL is larger than 120mA. The constant current driving method is suggested.

6.2 Internal Circuit Diagram



B/L Circuit

7. Packaging



8. Quality Assurance Specification

8.1 Conformity

The performance, function and reliability of the shipped products conform to the Product Specification.

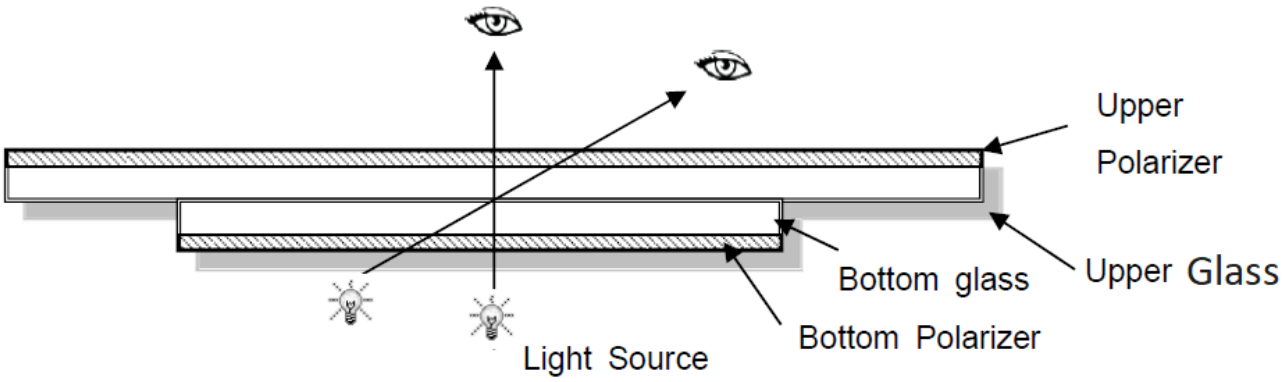
8.2 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	25 ± 5°C
Humidity:	65% ± 10% RH
Viewing Angle:	Normal Viewing Angle
Illumination:	Single fluorescent lamp (300 to 700 Lux)
Viewing distance:	30 - 50cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

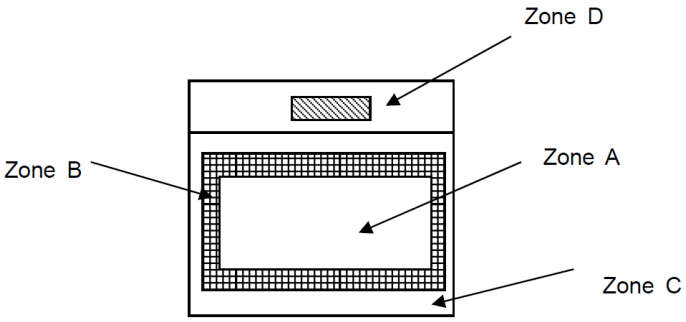


8.3 Delivery Assurance

8.3.1 Delivery Inspection Standards

Class II, Normal Inspection, ISO2859-1

8.3.2 Zone Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A + Zone B) Area which cannot be seen after assembly by customer.

Zone D: IC Bonding Area

Note: Generally, visual defects in Zone C can be ignored when it doesn't affect product function or appearance after assembly by customer

8.3.3 Criteria & Acceptable Quality Level

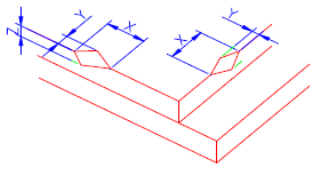
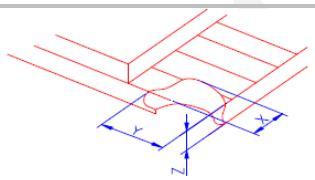
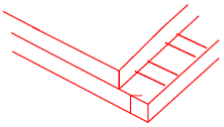
Major defect	Minor defect
0.65	1.5

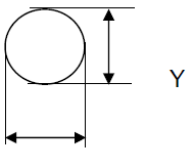
LCD: Liquid Crystal Display, TP: Touch Panel, LCM: Liquid Crystal Module

No.	Items	Criteria	Classification of defects
1	Functional defects	1) No display, open or miss line 2) Display abnormally 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot, Dim spot, Polarizer Bubble; Polarizer accidented spot.	
6	Soldering Appearance	Good soldering, Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

8.3.4 Criteria & Classification

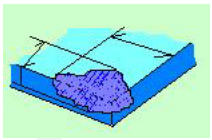
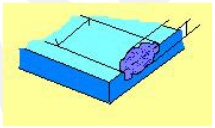
Units: mm

<table>
<tr><th>No</th><th>Item</th><th>Criteria</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>The edge of LCD broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤ 3</td><td>< Inner border line of the seal</td><td>≤ T</td></tr>
</table></td></tr>
<tr><td>LCD corner broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤ 3</td><td>< L</td><td>≤ T</td></tr>
</table></td></tr>
<tr><td>LCD crack</td><td> 
Crack Not allowed</td></tr>
</table>

<table>
<tr>
<td>2.0</td>
<td>Spot defect
 

Φ=(X+Y)/2</td>
<td>
1. light dot (LCD/TP/Polarizer black/white spot, light dot, pinhole, dent, stain)
<table>
<tr><th rowspan="2">Size</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.10<Φ≤0.25</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.25<Φ≤0.3</td><td colspan="2">2</td></tr>
<tr><td>Φ>0.35</td><td colspan="2">0</td></tr>
</table>
2. Dim spot （LCD/TP/Polarizer dim dot, light leakage、 dark spot）
<table>
<tr><th rowspan="2">Size</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.10<Φ≤0.25</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.25<Φ≤0.3</td><td colspan="2">2</td></tr>
<tr><td>Φ>0.35</td><td colspan="2">0</td></tr>
</table>
3. Polarizer accidented spot
<table>
<tr><th rowspan="2">Size</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.3<Φ≤0.5</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>Φ>0.5</td><td colspan="2">0</td></tr>
</table>
4. Pixel bad points （light dot， Dim dot, color dot）
<table>
<tr><th rowspan="2">Size</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.15<Φ≤0.25</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>Φ>0.3</td><td colspan="2">0</td></tr>
</table>
5. Polarizer Bubble
<table>
<tr><th rowspan="2">Size</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.3<Φ≤0.4</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.5<Φ≤0.6</td><td colspan="2">2</td></tr>
<tr><td>0.6<Φ</td><td colspan="2">0</td></tr>
</table>
</td>
</tr>
<tr>
<td>3.0</td>
<td>Line defect (LCD/ TP /Polarizer backlight black/white line,</td>
<td>
<table>
<tr><th>Width</th><th>Length</th><th>Acceptable Qty</th></tr>
</table>
</td>
</tr>
</table>

<table>
<tr><td></td><td>scratch, stain)</td><td>
<table>
<tr><th></th><th></th><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.07<W≤0.08</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>Electronic Components SMT</td><td>Not allow missing parts, solderless connection, cold solder joint, mismatch. The positive and negative polarity opposite</td></tr>
<tr><td>5.0</td><td>Display color& Brightness</td><td>1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples</td></tr>
<tr><td>6.0</td><td>LDC Mura</td><td>By 5% ND filter invisible.</td></tr>
<tr><td rowspan="4">7.0</td><td rowspan="4">CTP Related</td><td>CTP Cover sensor accidented black/white spot</td><td>
<table>
<tr><th rowspan="2">Size Φ</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.2</td><td colspan="2">3（distance≧10mm）</td></tr>
<tr><td>0.20<Φ≤0.25</td><td colspan="2">2</td></tr>
<tr><td>Φ＞0.3</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>CTP Cover scratch</td><td>
<table>
<tr><th rowspan="2">Width</th><th rowspan="2">Ignore (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="3">N≤3</td></tr>
<tr><td>0.07<W≤0.08</td><td>L≤3.0</td><td colspan="3">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>CTP Cover Pinhole/ Lack of ink</td><td>
<table>
<tr><th rowspan="2">Size</th><th>Acceptable Qty</th></tr>
<tr><th>C</th></tr>
<tr><td>Φ≤0.1</td><td>Ignore</td></tr>
<tr><td>0.1<Φ≤0.2</td><td>3(distance≧10mm)</td></tr>
<tr><td>0.25<Φ≤0.3</td><td>2</td></tr>
<tr><td>Φ>0.35</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>CTP Bonding bubble/ accidented</td><td>
<table>
<tr><th rowspan="2">Size</th><th colspan="2">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td rowspan="5"></td><td rowspan="5"></td><td>spot</td><td colspan="2"><table>
<tr><td>0.15<Φ≤0.2</td><td>3(distance≧10mm)</td></tr>
<tr><td>0.2<Φ≤0.25</td><td>2</td></tr>
<tr><td>Φ>0.25</td><td>0</td></tr>
</table></td></tr>
<tr><td>Assembly deflection</td><td colspan="2">beyond the edge of backlight ≤0.2mm</td></tr>
<tr><td>TP cover broken.
X：length
Y：width
Z：height</td><td><table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤0.5mm</td><td>Y≤0.5mm</td><td>Z<cover thickness</td></tr>
</table>Circuitry broken is not allowed.</td><td>  </td></tr>
<tr><td>TP cover broken.
X：length
Y：width
Z：height</td><td><table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤0.3mm</td><td>Y≤0.3mm</td><td>Z<LCD thickness</td></tr>
</table></td><td>  </td></tr>
</table>

No	Item	Criteria
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

8.4 Dealing with Customer Complaints

8.4.1 Non-conforming Analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.

After accepting it, Densitron should complete the analysis in reasonable time and update the status to the purchaser.

8.4.2 Handling of Non-conforming Displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

9. Reliability Specification

9.1 Reliability Tests

Test Item	Test Condition	Inspection after test
High Temperature Operation	70°C, 96 hours	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD. 2. non-display. 3. Missing segments/line. 4. Glass crack. 5. Current IDD is twice higher than initial value.
Low Temperature Operation	-20°C, 96 hours	
High Temperature Storage	80°C, 96 hours	
Low Temperature Storage	-30°C, 96 hours	
High Temperature & High Humidity Storage	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10°C, 30 min ↔ +60°C, 30 min, Change time: 5min 20CYC.	
ESD test	C=150pF, R=330, 5points/panel Air: ±8KV, 5times; Contact: ±6KV, 5 times. (Environment: 15°C ~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces, 80cm (MEDIUM BOX)	

Note 1: The test samples should be applied to only one test item.

Note 2: Sample size for each test item is 5~10 pieces.

Note 3: For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

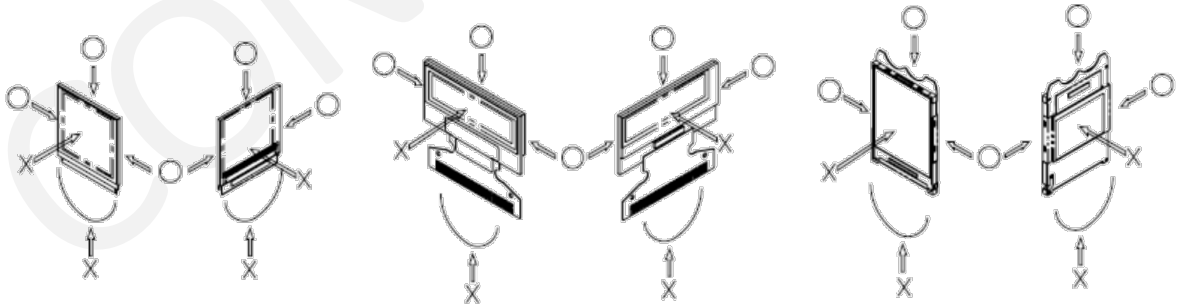
Note 5: Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

Note 6: The color fading mura of polarizing filter should not care.

10. Handling Precautions

10.1 Handling Precautions

1) Since the display panel is made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water
4) If pressure is applied to the display surface or its neighbourhood of the display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
5) The polarizer covering the surface of the display module is soft and easily scratched. Please be careful when handling the display module.
6) When the surface of the polarizer of the display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   a. Scotch Mending Tape No. 810 or an equivalent
   b. Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   c. Also, pay attention that the following liquid and solvent may spoil the polarizer:
      - Water
      - Ketone
      - Aromatic Solvents
7) Hold the display module very carefully when placing it into the system housing. Do not apply excessive stress or pressure to display module. And, do not over bend the film with electrode pattern layouts. These stresses will



influence the display performance. Also, secure sufficient rigidity for the outer cases.
8) Do not apply stress to the LSI chips and the surrounding molded sections.
9) Do not disassemble nor modify the display module.
10) Do not apply input signals while the logic power is off.
11) Pay sufficient attention to the working environments when handing display modules to prevent occurrence of element breakage accidents by static electricity.
    a. Be sure to make human body grounding when handling display modules.

b. Be sure to ground tools to use or assembly such as soldering irons.
c. To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
d. Protective film is being applied to the surface of the display panel of the display module. Be careful since static electricity may be generated when exfoliating the protective film.

12) A Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. If the display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
13) If electric current is applied when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

10.2 Storage Precautions

1) When storing display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you store these modules in the packaged state when they are shipped from Densitron) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the display module, when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

10.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for display module, and if these values are exceeded, panel damage may happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the display module, fasten the external plastic housing section.
7) If power supply to the display module is forcibly shut down by such errors as taking out the main battery while the display panel is in operation, we cannot guarantee the quality of this display module.

10.4 Operation Precautions

1) It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.
2) Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation.
3) Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged.
4) To protect display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the display modules.
   a. Pins and electrodes
   b. Pattern layouts such as the FPC
5) When the driver is being exposed (COG), semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if the driver is exposed to light, malfunctioning may occur.
   a. Design the product and installation method so that the driver may be shielded from light in actual usage.
   b. Design the product and installation method so that the driver may be shielded from light during the inspection processes.
6) Although the display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from the influences of noise on the system design.
7) We recommend you construct its software to make periodical refreshments of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

10.5 Cleaning Precautions

1) Keep TFT Scratch free: Avoid using abrasive materials like paper towels and newspaper in cleaning TFT LCD screens as they may scratch the surface. Instead, opt for a lint-free cloth. Don't spray the liquid directly on the monitor and remember to put gentle pressure when wiping the screen.

2) Avoid Vibration: During cleaning process, try to keep the TFT on shock proof platform to avoid strong shock and vibration. Do not apply pressure to the LCD screen of the LCD or bump or squeeze the LCD display back cover.

3) When the surface of the polarizer of the display module has soil, clean the surface. It takes advantage of using the following adhesion tape:

a) Scotch Mending Tape No. 810 or an equivalent.

b) Never try to breathe upon the soiled surface.

c) List of Safe and Unsafe solvents to clean TFT display:

Safe Solvents	Unsafe Solvents
Distilled Water	Ammonia
Isopropyl Alcohol	Acetone
Diluted White Vinegar = Water (Mix 1 part vinegar + 5 parts of Water)	Ethyl Alcohol
	Methyl Chloride
	Ethyl Acid

10.6 Other Precautions

1) Request the qualified companies to handle industrial wastes when disposing of the display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.