DMT040WVNMCMI-3B
PRODUCT SPECIFICATION

Version 0.1
Sep 01, 2023

Customer's Approval	
Signature	*Date*

Prepared by Yvette Hsieh
Approved by *Kenny Lin*

Revision History

VERSION	DATE	DESCRIPTION	AUTHOR
0.1	Sep 01, 2023	Preliminary	Yvette Hsieh

Legal Notice

Table of Contents

1. General Description

1.1 Introduction

This is a 3.97” size colour active matrix TFT LCD module that uses amorphous silicon TFT as a switching device. The display is normally black mode, transmissive, and featuring high contrast and excellent colour saturation. The resolution of the TFT-LCD is 480 x 800 and can display up to 16M colours. The display module supports 2 Lane MIPI interface.

1.2 Main Features

Item	Contents
Display Type	TFT LCD
Screen Size	3.97” Diagonal
Display Format	480 x RGB x 800 Dots
No. of Colour	16M
Overall Dimensions	60.14 (W) x 101.35 (H) x 3.265 (D) mm
Active Area	51.84 (W) x 86.4 (H) mm
Mode	Normally Black / Transmissive / IPS
Surface Treatment	Glare (7H)
Viewing Direction	All round
Interface	2 Lane MIPI
Driver IC	ILI9806E-2C
Backlight Type	LED, White, 8 chips
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
ROHS	Compliant to RoHS 2.0

1.3 Touch Features

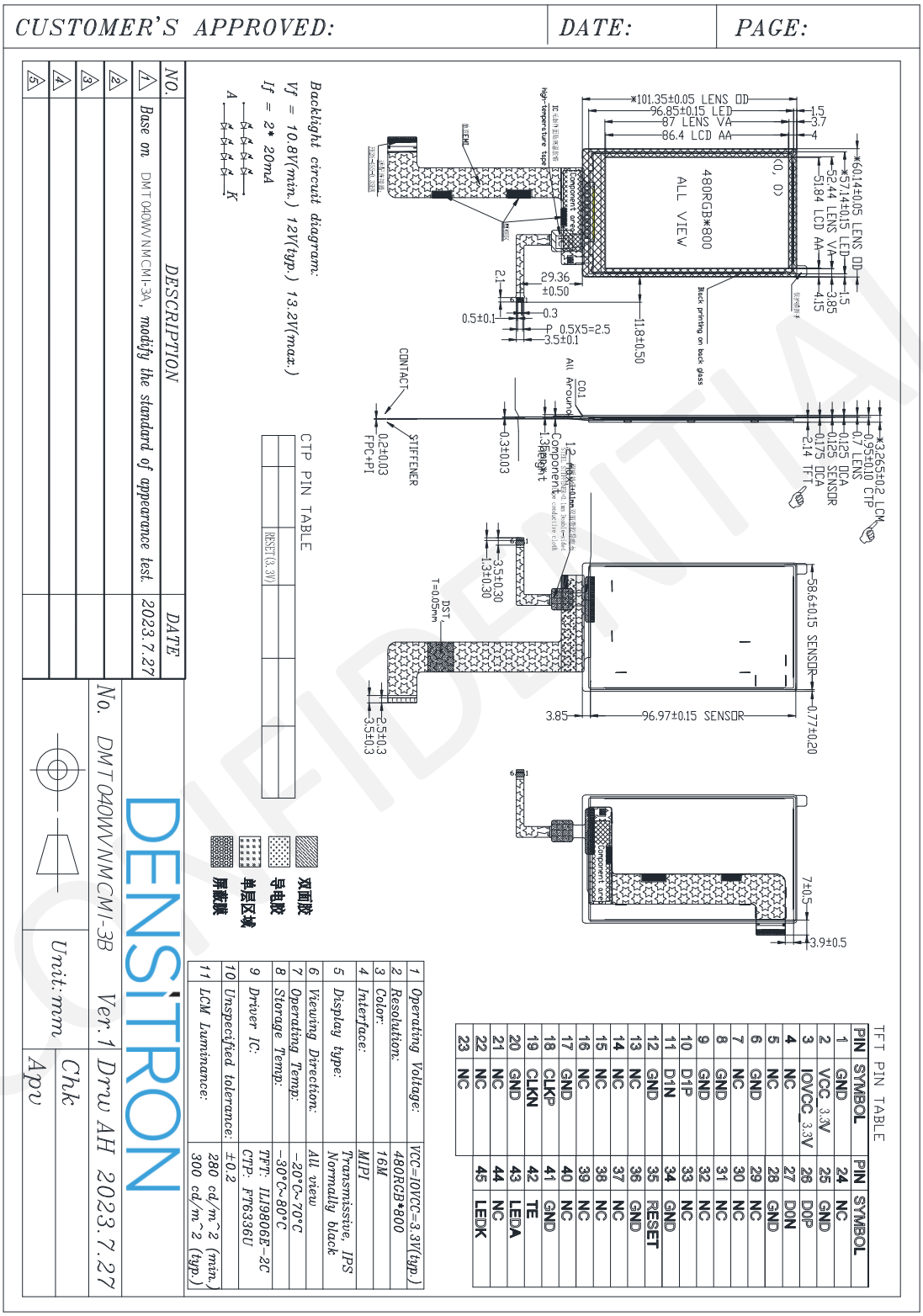
Item	Contents
Touch Panel	CTP
Touch Technology	Mutual capacitor
Bonding Type	Optical Bonding
Input Method	Finger
Touch Point	5 Point
Positional Accuracy	2.5mm at 4 edges and 1.5mm at center (mm)
Cover glass	Soda lime glass, chemically hardened
Hardness	6H
Surface treatment	No
Optical transmittance	87%
Touch controller	FT6336U
Interface to Host	I^2C
Slave Address	0X70
Connection Type	ZIF Connector
The program name	MTP397-004AAAMFIL_ FT6x36_Ver0x19_20220531_all.bin

2. Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Display Format	480 x RGB x 800	Dots
Overall Dimensions	60.14 (W) x 101.35 (H) x 3.265 (D)	mm
Active Area	51.84 (W) x 86.4 (H)	mm
Dot Pitch	0.108 (W) x 0.108 (H)	mm
Weight	38.4g	g
IC Controller/Driver	ILI9806E-2C	

2.2 Mechanical Drawing



3. Electrical Specification

3.1 Absolute Maximum Ratings

AGND = GND = 0V, Ta = 25℃

Item	Symbol	Min	Max	Unit	Note
Power Voltage	VCC	-0.3	4.6	V	-
	IOVCC	-0.3	4.6	V	-
Operating Temperature	T_{OP}	-20	+70	°C	-
Storage Temperature	T_{ST}	-30	+80	°C	-

Note 1: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. For normal operations, it is desirable to use this module under the conditions according to Section 3.2 “Electrical Characteristics”, to avoid malfunctioning.

Note 2: Background colour changes slightly depending on ambient temperature. This phenomenon is reversible.

Note 3: Please refer to item of RELIABILITY.

3.2 Electrical Characteristics

3.2.1 Recommended Operating Condition

(AGND = GND = 0V, Ta = 25℃)

Item	Symbol	Min	Typ.	Max	Unit	Note
Power Voltage	VCC	2.5	3.3	3.6	V	-
	IOVCC	1.65	3.3	3.6	V	-
Input Logic High Voltage	Vih	0.7IOVCC	-	IOVCC	V	-
Input Logic Low Voltage	Vil	-0.3	-	0.3IOVCC	V	-

3.2.2 DC Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Power & Operation Voltage							
Operating Voltage	VCI VCIP VCIR	-	2.5	3.3	3.6	V	-
Operating Voltage	IOVCC	-	1.65	3.3	3.6	V	1, 2
OTP Supply Voltage	VPP	-	-	5.0	-	V	1
Logic High Level Input Voltage	VIH	-	0.7*IOVCC	-	IOVCC	V	1
Logic Low Level Input Voltage	VIL	-	-0.3	-	0.3*IOVCC	V	1
Logic High Level Output Voltage TE, SDO (SDA), LEDPWM	VOH	IOH=-1.0mA	0.8*IOVCC	-	IOVCC	V	1
Logic Low Level Output Voltage TE, SDO (SDA), LEDPWM	VOL	IOL=+1.0mA	0	-	0.2*IOVCC	V	1
Gate Driver High Voltage	VGH	-	10.0	-	20	V	-
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	-
Driver Supply Voltage	-	$\|VGH - VGL\|$	16	-	32	V	-
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.0	-	0	V	3
Source Driver							
Source Output Range	VSOUT	-	VREG2OUT+0.1	-	VREG1OUT-0.1	V	4

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Positive Gamma Reference Voltage	VREG1OUT	-	3.0	-	6.1875	V	5
Negative Gamma Reference Voltage	VREG2OUT	-	-6.1875	-	-3.0	V	5
Source Output Setting Time	Tr	Below with 99% precision	-	15	20	Us	3, 4
Output Deviation Voltage (Source Output Channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	30	mV	3
		4.2V>Sout>0.8V	-	-	20	mV	-
Output Offset Voltage	VOFFSET	-	-	-	35	mV	3
Booster Operation							
Booster Voltage	DDVDH	-	-	-	6.5	V	-
Booster Voltage	DDVDL	-	-6.5	-	-	V	-
Booster Drop Voltage	DDVDH drop	Loading=1mA	-	-	5	%	-
Gate Driver High Voltage	VGH	-	10.0	-	20	V	-
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	-
Standby Mode Current Consumption							
Sleep In Mode	I (IOVCC SLP IN)	Ta=25℃ VCI=2.8V IOVCC=1.8V	0	-	10	uA	-
	I (VCI SLP IN for DPI+SPI I/F)		5	-	60	uA	-
	I (VCI SLP IN for MIPI DSI I/F)		5	-	60	uA	-

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Deep Standby Mode	I (IOVCC DSTB)		0	-	1	uA	-
	I (VCI DSTB)		0	-	1	uA	-

Note 1: Ta = -30 to 70 °C (to 85 °C no damage), IOVCC=1.65V to 3.6V, VCIP=2.5V to 3.6V.

Note 2: Supply digital IOVCC voltage equal or less than analog VCIP voltage.

Note 3: Source channel loading = 10pF/channel

Note 4: The Max. Value is between with Note 3 measure point and Gamma setting value

Note 5: VREG1OUT≦DDVDH-0.3V and VREG2OUT≧DDVDL+0.3V.

3.3 Interface Pin Assignment

3.3.1 TFT PIN Define

No.	Symbol	I/O	Function
1	GND	P	Ground
2	VCC_3.3V	P	Power supply for analog system
3	IOVCC_3.3V	P	Power supply for I/O block.
4	NC	-	No connection
5	NC	-	No connection
6	GND	P	Ground
7	NC	-	No connection
8	GND	P	Ground
9	GND	P	Ground
10	D1P	I/O	MIPI DSI differential data pair (DSI-Dn+/-).
11	D1N	I/O	MIPI DSI differential data pair (DSI-Dn+/-).
12	GND	P	Ground
13	NC	-	No connection
14	NC	-	No connection
15	NC	-	No connection
16	NC	-	No connection
17	GND	P	Ground
18	CLKP	I	MIPI DSI differential clock pair (DSI-CLK+/-).
19	CLKN	I	MIPI DSI differential clock pair (DSI-CLK+/-).
20	GND	P	Ground
21	NC	-	No Connection

No.	Symbol	I/O	Function
22	NC	-	No Connection
23	NC	-	No Connection
24	NC	-	No Connection
25	GND	P	Ground
26	D0P	I/O	MIPI DSI differential data pair (DSI-Dn+/-).
27	D0N	I/O	MIPI DSI differential data pair (DSI-Dn+/-).
28	GND	P	Ground
29	NC	-	No Connection
30	NC	-	No Connection
31	NC	-	No Connection
32	NC	-	No Connection
33	NC	-	No Connection
34	GND	P	Ground
35	RESET	I	The external reset input.
36	GND	P	Ground
37	NC	-	No Connection
38	NC	-	No Connection
39	NC	-	No Connection
40	NC	-	No Connection
41	GND	P	Ground
42	TE	O	Tearing effect output
43	LEDA	P	LED anode
44	NC	-	No connection
45	LEDK	P	LED cathode

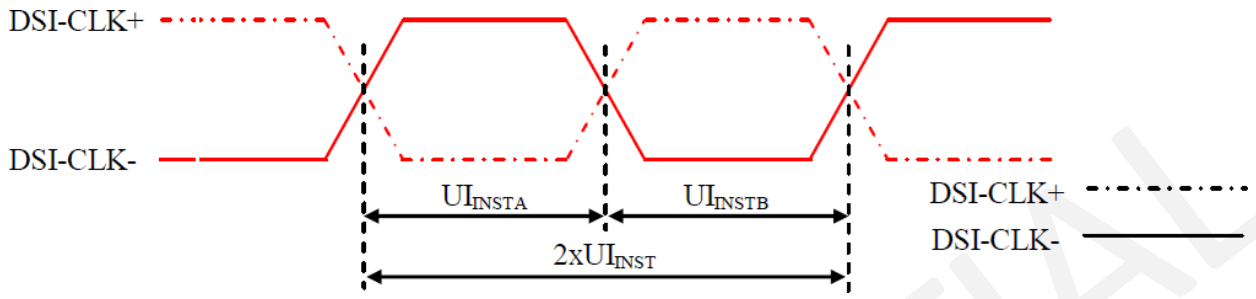
3.3.2 CTP Pin Define

No.	Symbol	I/O	Function
1	GND	P	Ground
2	VDD_3.3V	P	Supply voltage
3	RESET (3.3V)	I	External Reset, Low active
4	EINT (3.3V)	O	External interrupt to the host
5	SCL (3.3V)	I	I^2C clock input
6	SDA (3.3V)	I/O	I^2C data input and output

3.4 Timing Characteristics

3.4.1 AC Electrical Characteristics

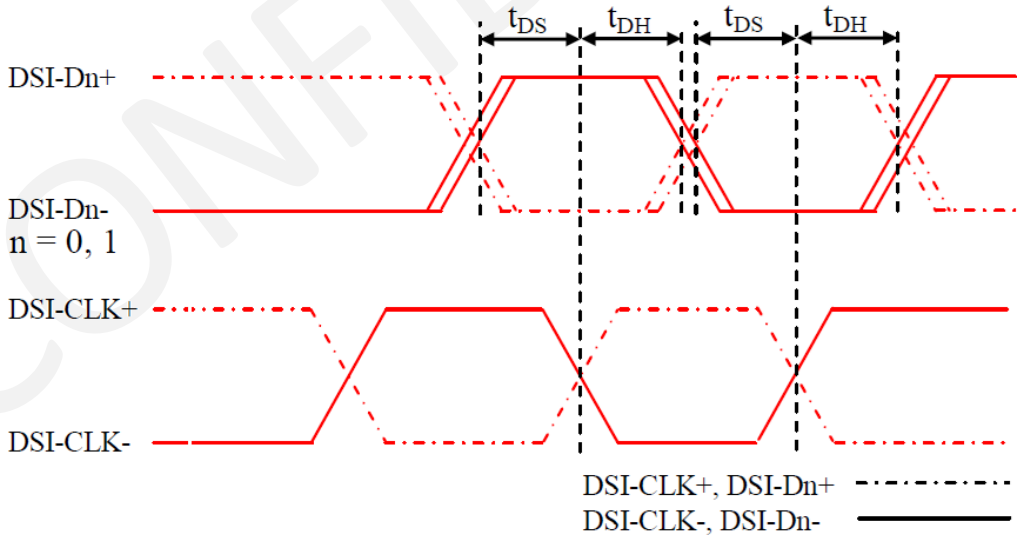
3.4.1.1 High Speed Mode – Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

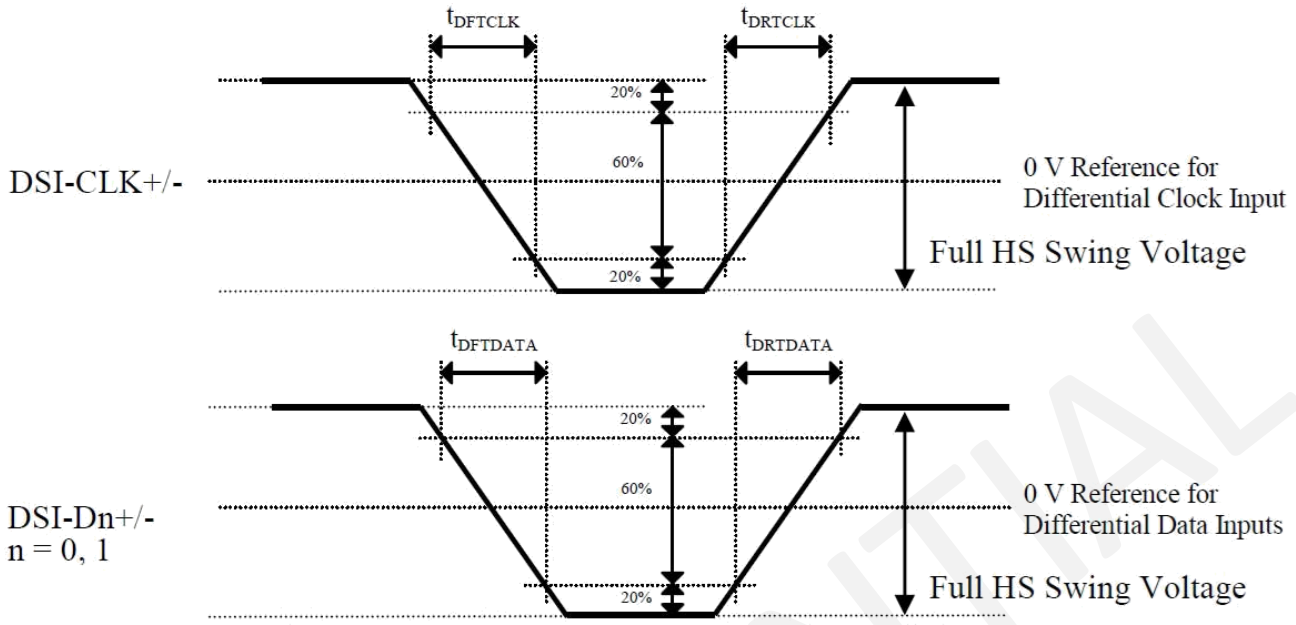
Note: $UI=UI_{INSTA}=UI_{INSTB}$

3.4.1.2 High Speed Mode – Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-	-

3.4.1.3 High Speed Mode – Rise and Fall Timings



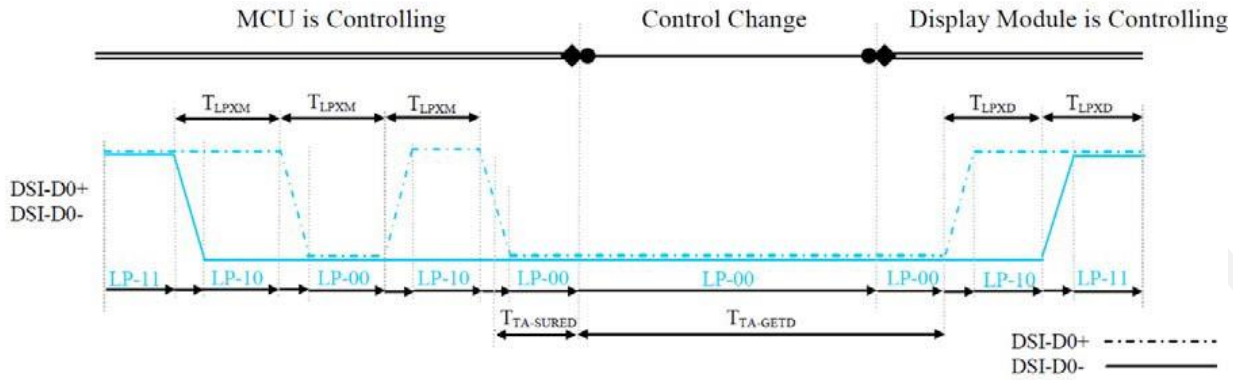
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	-	-	150	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	-	-	150	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150	ps

Note: The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard.

3.4.1.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (ILI9806E) sequence below.

Figure: BTA from the MPU to the Display Module



Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (ILI9806E) to the MPU sequence below.

Figure: BTA from the Display Module to the MPU

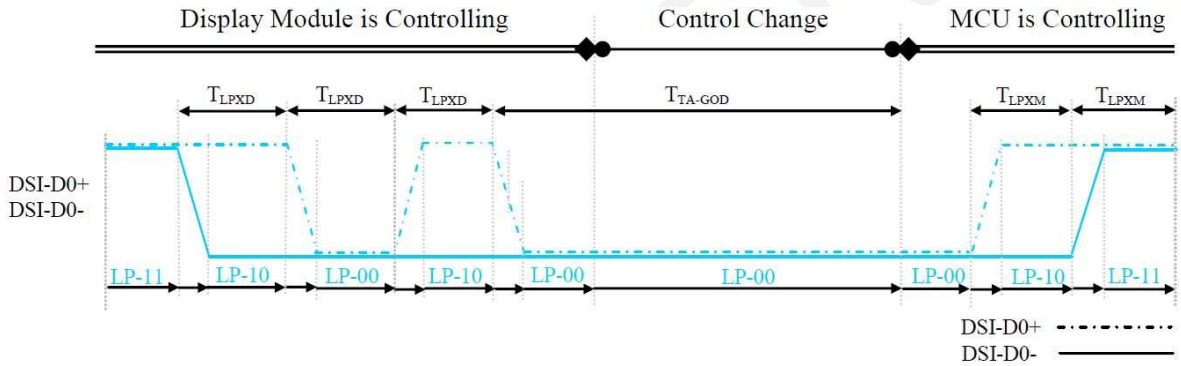


Table: Low Power State Period Timings – A Table

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU ➔ Display Module (ILI9806E)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9806E) ➔ MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (ILI9806E) starts driving	T_{LPXD}	2 x T_{LPXD}	ns

Table: Low Power State Period Timings – B Table

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9806E)	5 x T_{LPXD}	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	4 x T_{LPXD}	ns

3.4.1.5 Data Lanes from Low Power Mode to High Speed Mode

Figure: Data Lanes – Low Power Mode to High Speed Mode Timings

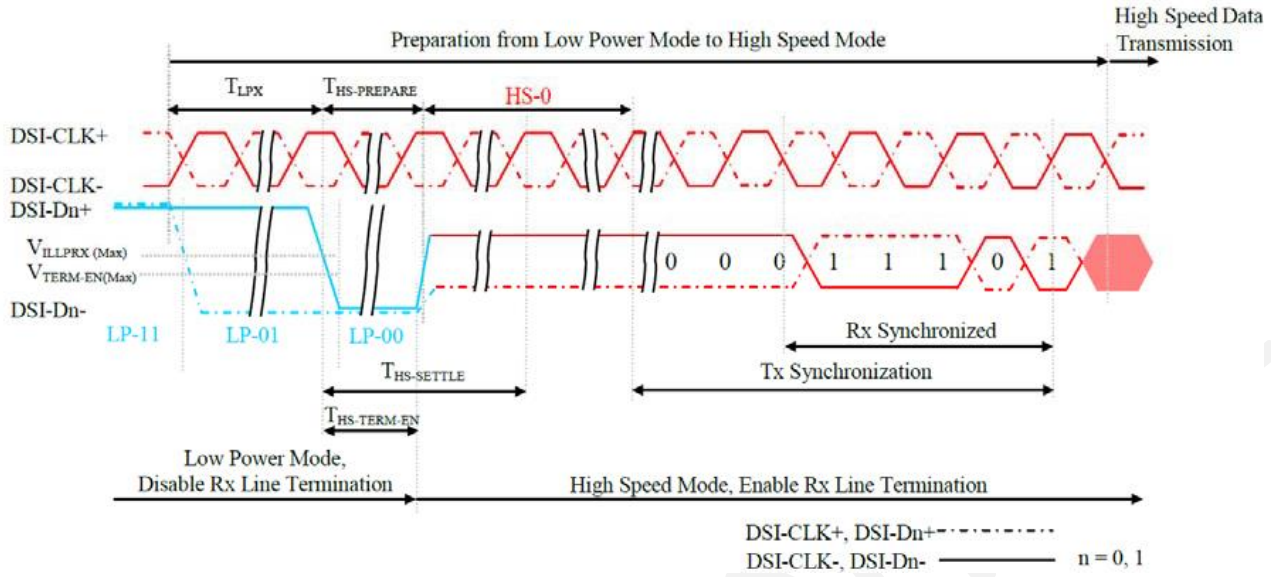


Table: Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

3.4.1.6 Data Lanes from High Speed Mode to Low Power Mode

Figure: Data Lanes – High Speed Mode to Low Power Mode Timings

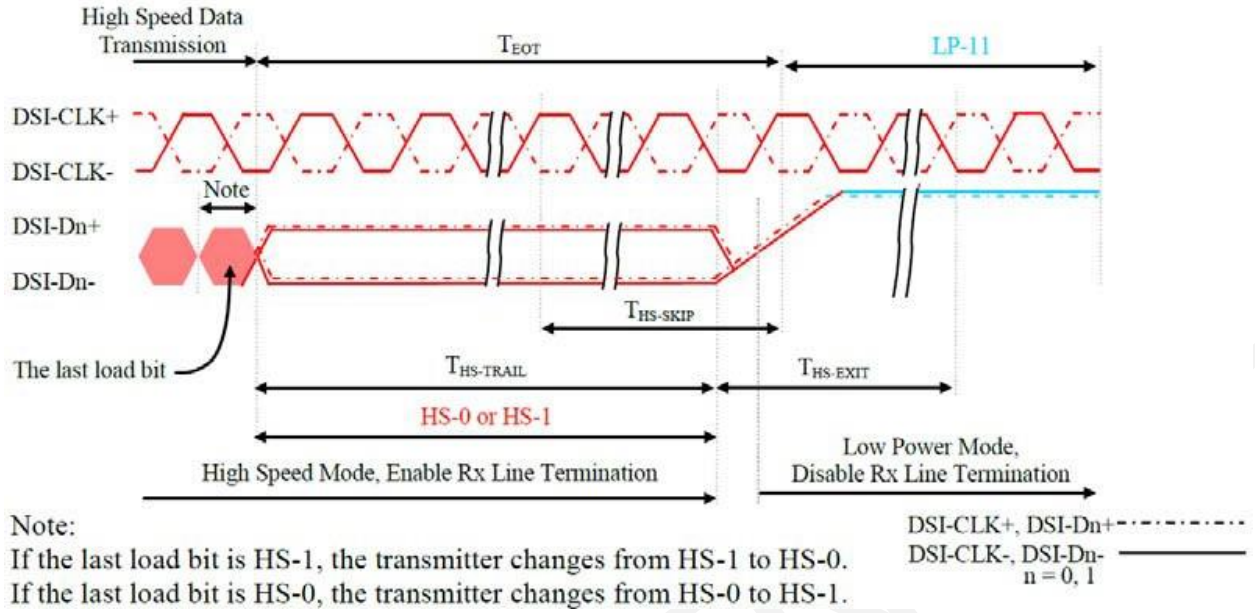


Table: Data Lanes – High Speed Mode to Low Power Mode Timings Table

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9806E) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

3.4.1.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

Figure: Clock Lanes – High Speed Mode to/from Low Power Mode Timings

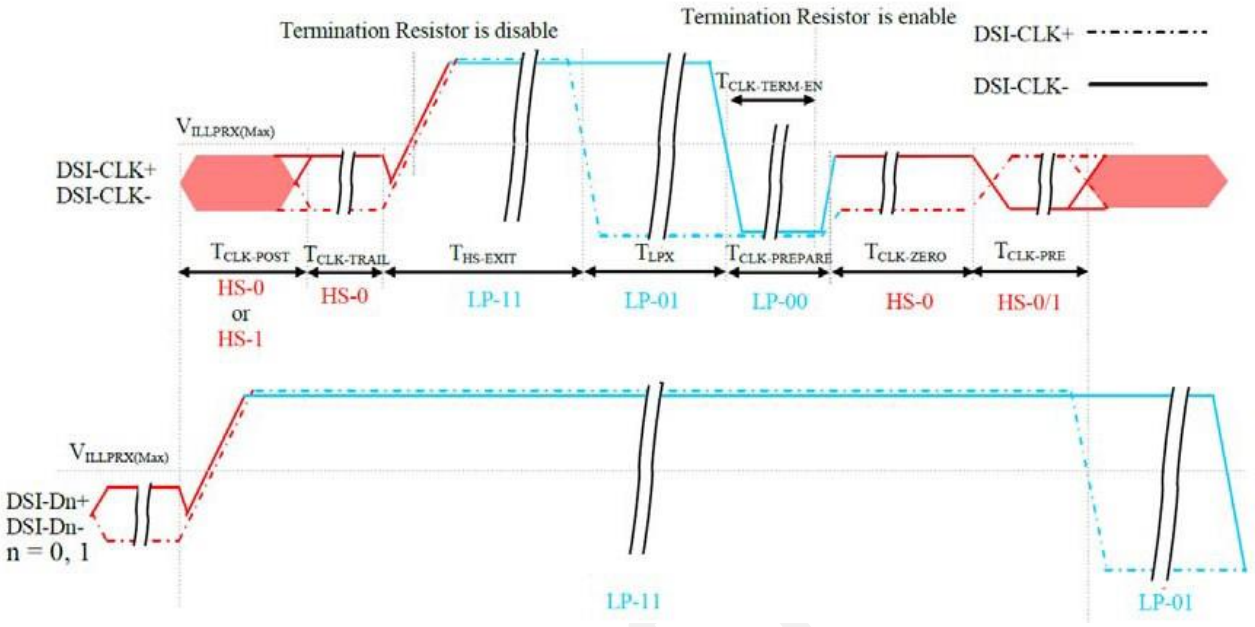


Table: Clock Lanes – High Speed Mode to/from Low Power Mode Timings Table

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

3.4.1.8 DSI DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

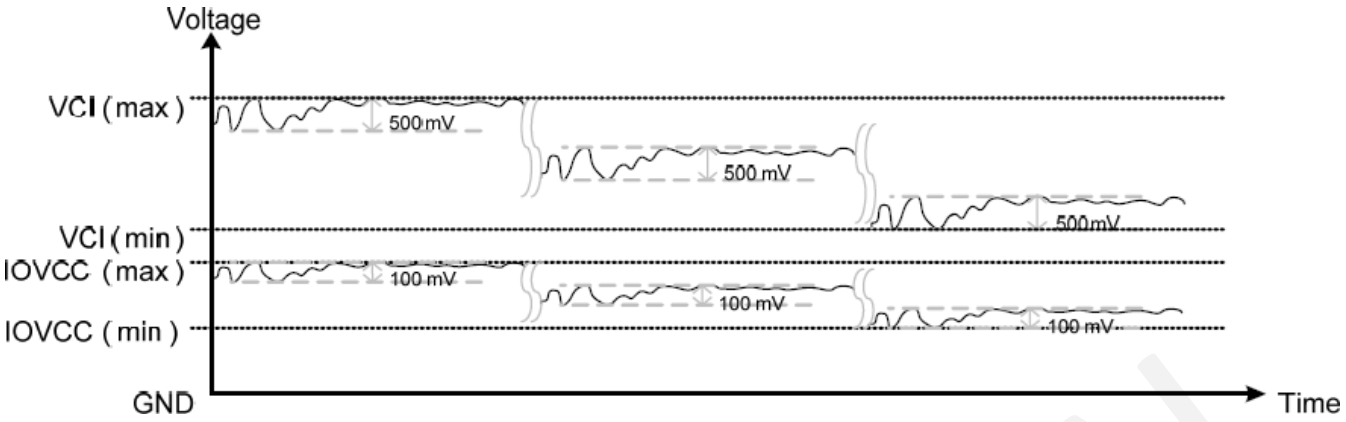
3.4.1.9 DC Characteristics for Power Lines

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Analog Power Supply Voltage	VCI	Operating Voltage	2.5	3.3	3.6	V	-
Digital Power Supply Voltage	IOVCC	I/O Supply Voltage	1.65	3.3	3.6	V	-
Analog Power Supply Voltage Noise	VVCI_NOISE	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV	-
		Noise Range, 0 to 30KHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV	-
I/O Power Supply Voltage Noise	VIOVCC_NOISE	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV	-

Note 1: Ta=-30℃ to 70℃ (to +85℃ no damage)

Note 2: These values are not symmetric amplitude, which centersm3g points are IOVCC or VCI. See examples as reference purposes, when VVCI_NOISE and VIOVCC_NOISE are maximums, below.

Figure: Noise on Power Supply Lines



3.4.1.10 DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP- TX is mentioned on the condition column. Other logical levels of the table are for MPU interface.

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Logic High level output voltage	VOH	IOUT=-1mA	0.8VVCI	-	VVCI	V	2
Logic Low level output voltage	VOL	IOUT=-1mA	0.0	-	0.2VVCI	V	2
Logic High level input voltage	VIHLPCD	LP-CD	450	-	1350	mV	3
Logic Low level input voltage	VILLPCD	LP-CD	0.0	-	200	mV	3
Logic High level input voltage	VIHLPRX	LP-RX (CLK, D0, D1)	880	-	1350	mV	3
Logic Low level input voltage	VILLPRX	LP-RX (CLK, D0, D1)	0.0	-	550	mV	3
Logic Low level input voltage	VILLPRXULP	LP-RX (CLK ULP Mode)	0.0	-	300	mV	3
Logic High level output current	VOHLPTX	LP-TX (D0)	1.1	-	1.3	V	3
Logic Low level output current	VOLLPTX	LP-TX (D0)	-50	-	50	mV	3
Logic High Level Input Current	IIH	LP-CD, LP-RX	-	-	10	uA	3
Logic Low Level Input Current	IIL	LP-CD, LP-RX	-10	-	-	uA	3

Note 1: Ta=-30℃ to 70℃ (to +85℃ no damage)

Note 2: LEDPWM

Note 3: DSI High Speed mode is off

3.4.1.11 DC Characteristics for DSI HS Mode

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Input Common Mode Voltage for Clock	VCMCLK	DSI-CLK+/-	70	-	330	mV	2,3
Input Common Mode Voltage for Data	VCMDATA	DSI-Dn+/-	70	-	330	mV	2, 3, 5
Common Mode Ripple for Clock Equal or Less than 450MHz	VCMRCLKL450	DSI-CLK+/-	-50	-	50	mV	4
Common Mode Ripple for Data Equal or Less than 450 MHz	VCMRDATAL450	DSI-Dn+/-	-50	-	50	mV	4, 5
Common Mode Ripple for Clock More than 450 MHz (peak sine wave)	VCMRCLKM450	DSI-CLK+/-	-	-	100	mV	-
Common Mode Ripple for Data More than 450 MHz (peak sine wave)	VCMRDATAM450	DSI-Dn+/-	-	-	100	mV	5
Differential Input Low Level Threshold Voltage for Clock	VTHLCLK-	DSI-CLK+/-	-70	-	-	mV	-
Differential Input Low Level Threshold Voltage for Data	VTHLDATA	VTHLDATADSI-Dn+/-	-70	-	-	mV	5
Differential Input High Level Threshold Voltage for Clock	VTHHCLK+	DSI-CLK+/-	-	-	70	mV	-
Differential Input High Level Threshold Voltage for Data	VTHHDATA+	DSI-Dn+/-	-	-	70	mV	5
Single-ended Input Low Voltage	VILHS	DSI-CLK+/-, DSI-Dn+/-	-40	-	-	mV	3, 5
Single-ended Input High Voltage	VIHHS	DSI-CLK+/-, DSI-Dn+/-	-	-	460	mV	3, 5
Differential Termination Resistor	RTERM	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω	5
Single-ended Threshold Voltage for Termination Enable	VTERM-EN	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV	5

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Termination Capacitor	CTERM	DSI-CLK+/-, DSI-Dn+/-	-	-	60	pF	5, 6

Note 1: Ta = -30℃ to 70℃ (to +85℃ no damage), IOVCC = 1.65 to 1.95V.

Note 2: Includes 50mV (-50mV to 50mV) ground difference.

Note 3: Without VCMRCLKM450/VCMRDATAM450.

Note 4: Without 50mV (-50mV to 50mV) ground difference.

Note 5: n = 0 and 1.

Note 6: For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

3.4.2 Power On/Off Sequence

IOVCC and VCI can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VCI and IOVCC can be powered down with minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

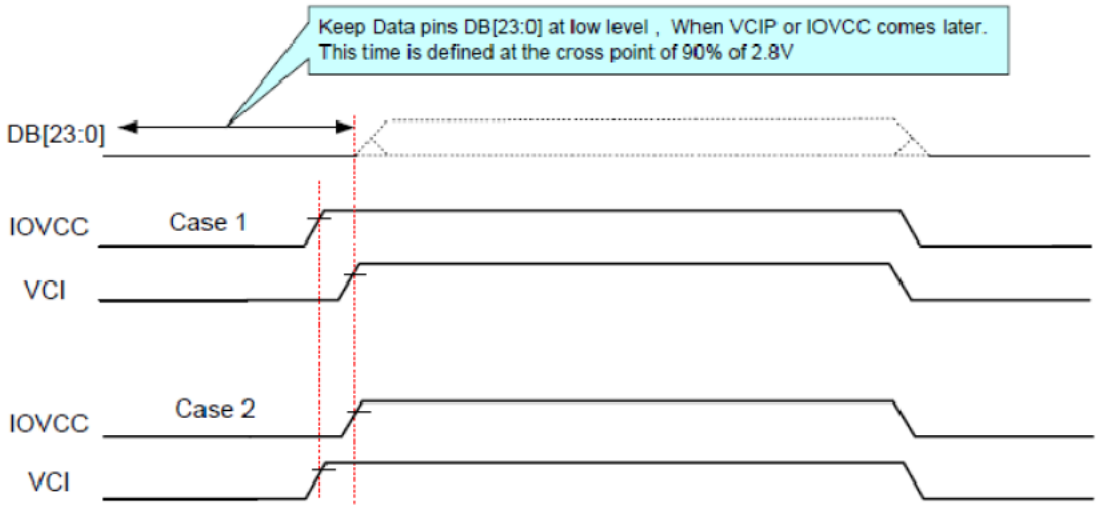
Note 1: There will be no damage to ILI9806E if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

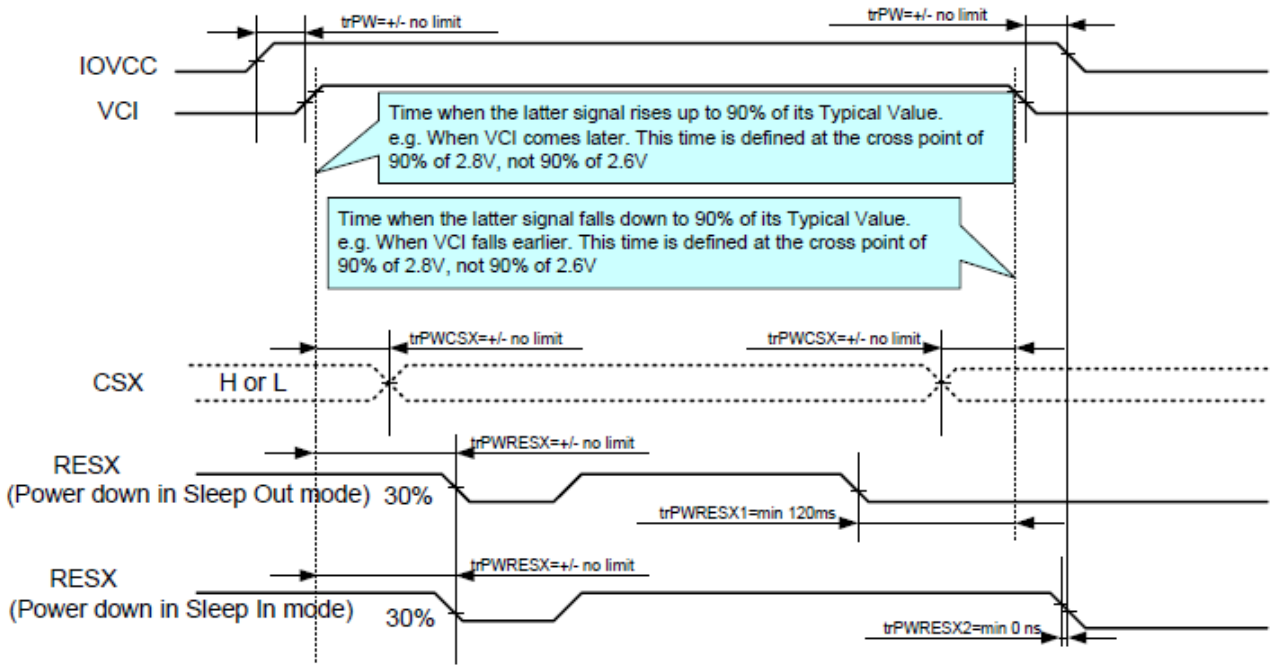
Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.1 and 7.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

Note 5: Keep data pins DB[23:0] at low level, when VCIP or IOVCC comes later



Case 1 –RESX line is held High or Unstable by Host at Power ON

If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

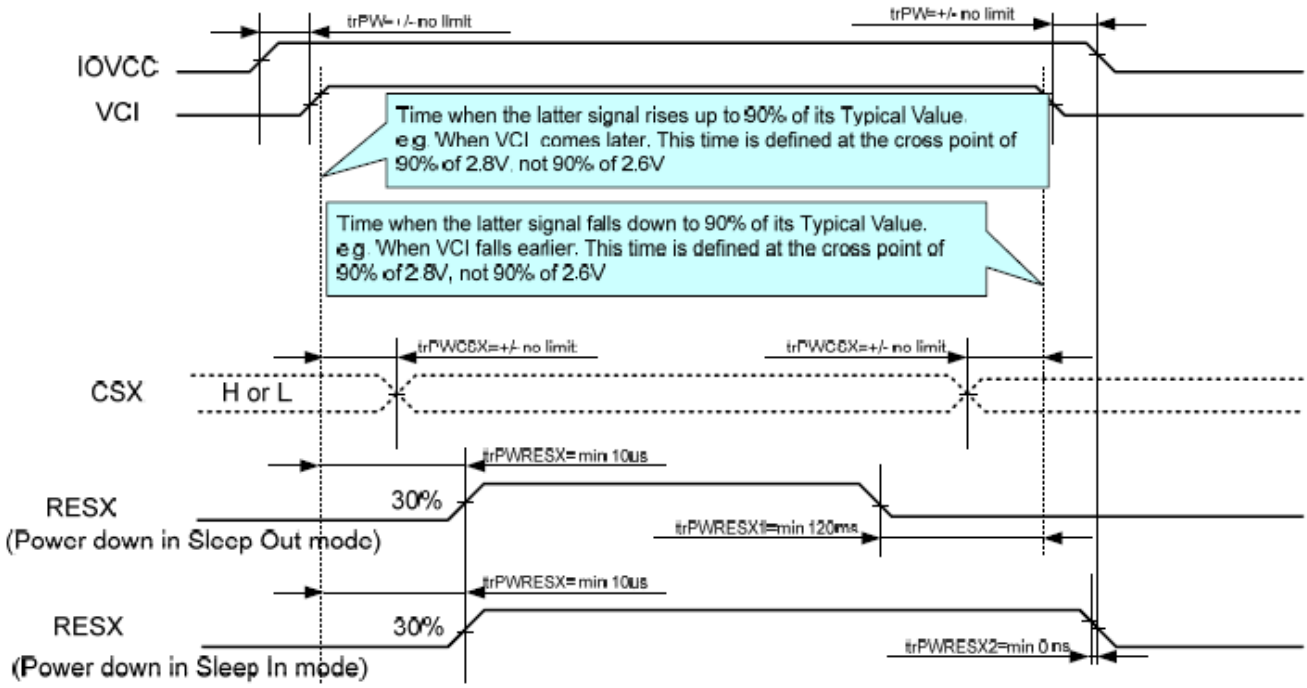


trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

Case 2 – RESX line is held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

4. Optical Specification

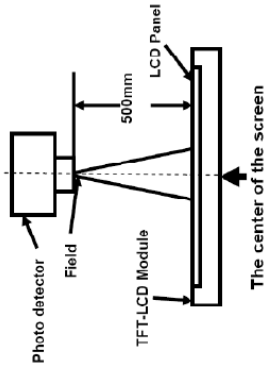
4.1 Optical Characteristics

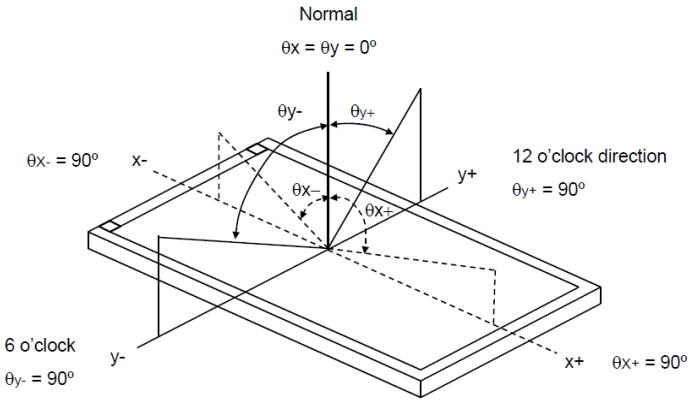
Characteristics		Symbol	Conditions	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	θ = 0° Normal viewing angle	720	900	-	-	1, 3
Response time		TR + TF		-	35	45	ms	1, 4
Viewing Angle	Left	θ_x-	CR>10	-	80	-	deg	2
	Right	θ_x+		-	80	-		
	Up	θ_Y+		-	80	-		
	Down	θ_Y-		-	80	-		
Colour Chromaticity	Red	Rx	θ = 0° Normal viewing angle	0.593	0.633	0.673	-	1, 5
		Ry		0.294	0.334	0.374		
	Green	Gx		0.286	0.326	0.366		
		Gy		0.577	0.617	0.657		
	Blue	Bx		0.111	0.151	0.191		
		By		0.008	0.048	0.088		
	White	Wx		0.261	0.301	0.341		
		Wy		0.283	0.323	0.363		
Luminance		Lv	I_F = 40mA	280	300	-	cd/m^2	5
Uniformity		Avg	-	70	-	-	%	5

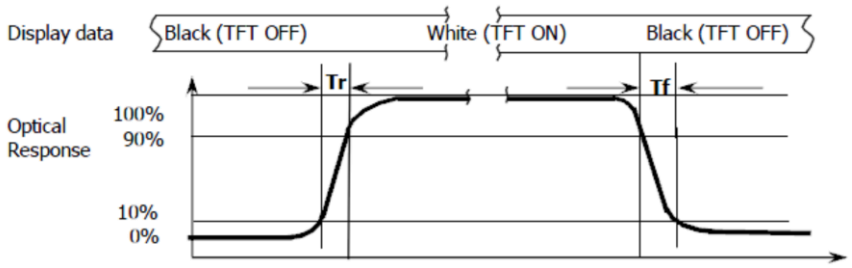
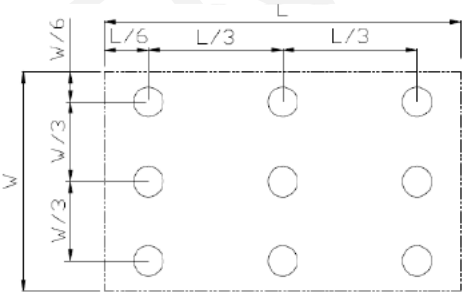
Conditions:

1. If=40mA(Backlight current), VCC = 3.3V, the ambient temperature is 25°C.

2. The test systems refer to Note 2.

<table>
<tr><th>Note</th><th>Item</th><th>Test method</th></tr>
<tr><td>1</td><td>Definition of optical measurement system</td><td>The optical characteristics should be measured in dark room. After 5Minutes operation, the optical properties are measured at the center point of the LCD screen. ALL input terminals LCD panel must be ground when measuring the center area of the panel.
 

<table>
<tr><th>Item</th><th>Photo detector</th><th>Field</th></tr>
<tr><td>Contrast Ratio</td><td rowspan="2">CS1000</td><td rowspan="2">1°</td></tr>
<tr><td>Luminance
Lum Uniformity</td></tr>
<tr><td>Chromaticity</td><td>CS1000</td><td></td></tr>
<tr><td>Response Time</td><td>DMS703</td><td>-</td></tr>
</table></td></tr>
<tr><td>2</td><td>Definition of Viewing Angle (θx, θy)</td><td>Viewing angle is measured at the center point of the LCD by CONOSCOPE (DMS703)
 
</td></tr>
<tr><td>3</td><td>Definition of Contrast Ratio (CR)</td><td>White state: The state is that the LCD should drive by Vwhite.
Contrast ratio (CR) = Luminance measured when LCD is at “white state” / Luminance measured when LCD is at “black state”
Black state: The state is that the LCD should drive by Vblack.
Vwhite: To be determined Vblack: To be determined</td></tr>
<tr><td>4</td><td>Definition of Response Time (T_R, T_F)</td><td>The response time is defined as the LCD optical switching time interval between “White”state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%.And fall time (TOFF)is the time between photo detector output intensity changed from 10% to90%.</td></tr>
</table>

Note	Item	Test method
		
5	Definition of color chromaticity （CIE1931）	Color coordinates measured at center point of LCD.
6	Definition of Luminance Uniformity	Active area is divided into 9 measuring areas(Refer Fig.2).Every measuring point is placed at the center of each measuring area. Luminance Uniformity (U)=Lmin/Lmax L-Active area length W-Active area width  L max: The measured Maximum luminance of all measurement position. L min: The measured Minimum luminance of all measurement position.
7	Definition of luminance	Measure the luminance of white state at center point.

5. LED Backlight Specification

5.1 LED Backlight Characteristics

Ta = 25℃

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Forward Voltage	V_F	-	10.8	12	13.2	V	-
Forward Current	I_F	-	-	40	-	mA	-
Operating Life Time	-	-	36000	-	-	Hours	1, 2

Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: If the module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.

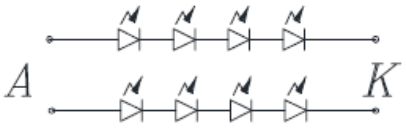
Note 3: Operating life means brightness goes down to 50% initial brightness. Minimum operating life time is estimated data.

5.2 INTERNAL CIRCUIT DIAGRAM

Backlight circuit diagram:

Vf = 10.8V(min.) 12V(typ.) 13.2V(max.)

If = 2 20mA*



6. Packaging

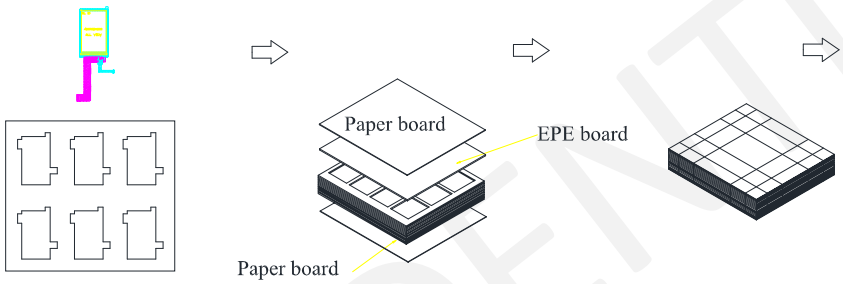
CUSTOMER'S APPROVED:	2021.06.17	PAGE: 1 1

PACKLING ORDER:

1) Putting 6 pcs Modules on each EPE tray.

2) Putting 7 pcs EPE trays together with EPE paper on the top of EPE tray.

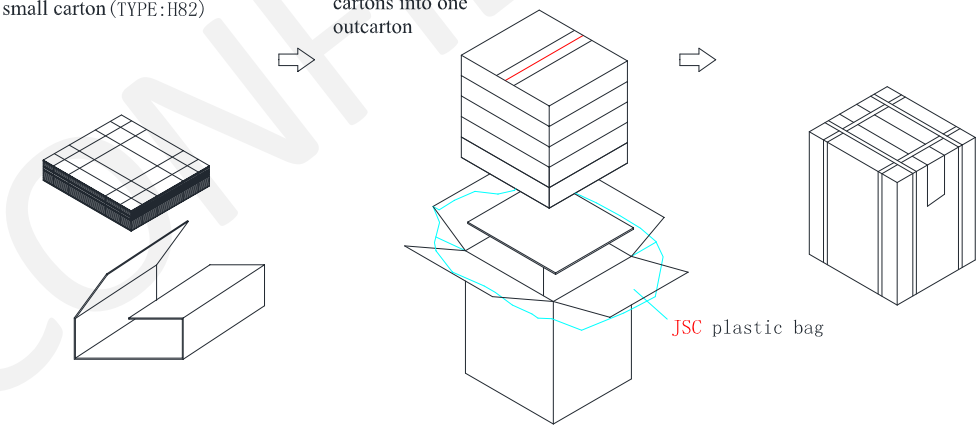
3) Assembling the boards and the tray together with adhesive tape



4) Putting in the inner small carton (TYPE:H82)

5) Putting 5 small cartons into one outcarton

6) Packing finished



Note: 6 pcs in a tray, 7 trays in a inner carton, 5 inner cartons in a out carton, so 6x7x5=210pcs/Outcarton

Dimension (Small carton): 385*325*87mm Dimension (Out carton): 394*344*470mm

7. Quality Assurance Specification

7.1 Conformity

The performance, function and reliability of the shipped products conform to the Product Specification.

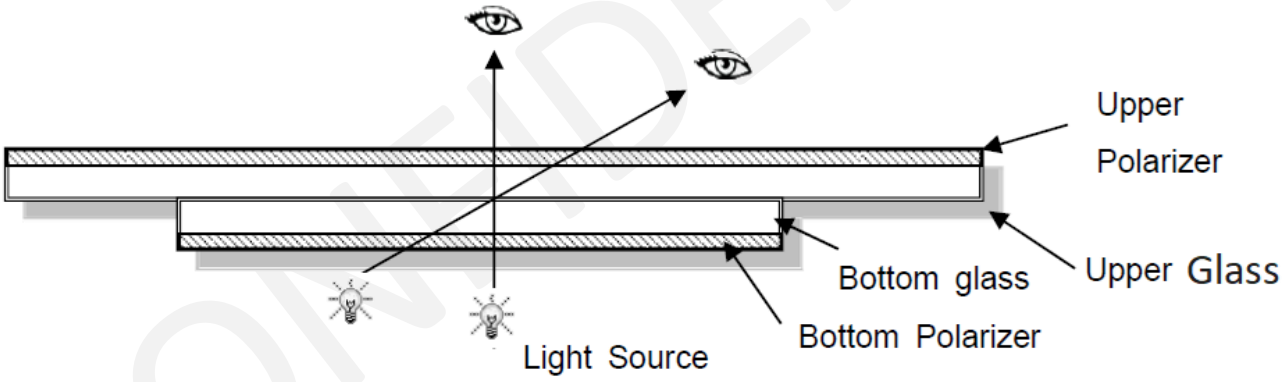
7.2 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	25 ± 5°C
Humidity:	65% ± 5% RH
Viewing Angle:	Normal Viewing Angle
Illumination:	under 40W fluorescent light
Viewing distance:	35± 5cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

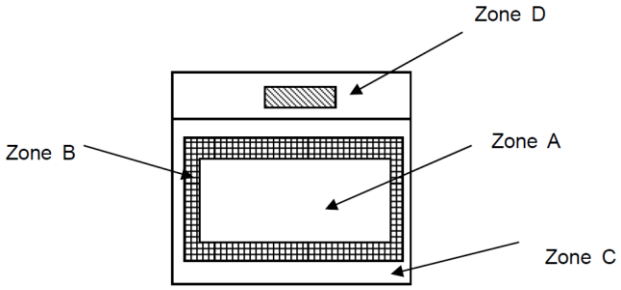


7.3 Delivery Assurance

7.3.1 Delivery Inspection Standards

Class II, Normal Inspection, MIL-STD-105E

7.3.2 Zone Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A + Zone B) Area which cannot be seen after assembly by customer.

Zone D: IC Bonding Area

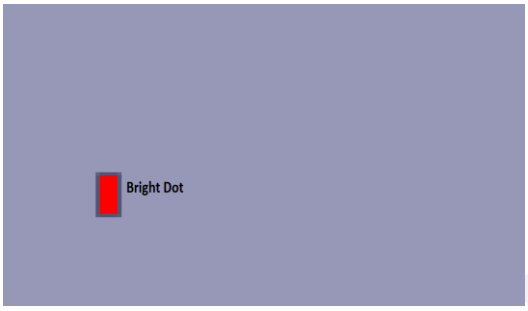
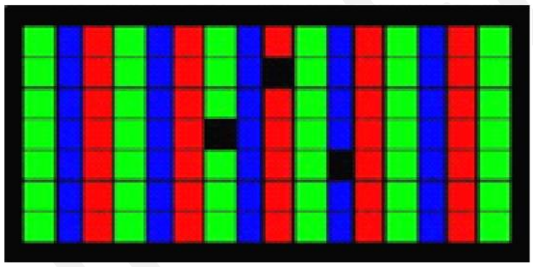
Note: Generally, visual defects in Zone C can be ignored when it doesn't affect product function or appearance after assembly by customer

7.3.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major (MA)	0.65	1. Liquid crystal leakage 2. Wrong polarizer 3. Outside dimension 4. Bright dot, dark dot 5. Display abnormal 6. Class crack
Minor (MI)	1.0	1. Spot Defect (Including black spot, white spot, pinhole, foreign particle, bubbles, hurt) 2. Fragment 3. Line Defect (Including black line, white line, scratch) 4. Incision defect 5. Newton's ring 6. Other visual defects

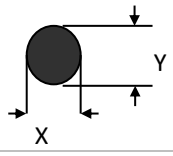
7.3.4 Criteria & Classification

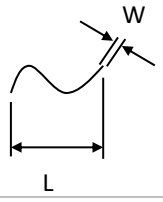
7.3.4.1 Bright/ Dark Dots Explain

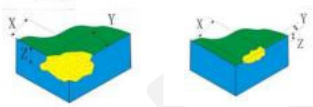
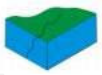
Name	Explain	Definition
Bright dot	Dots bright and unchanged in size in which LCD panel is displaying black pattern 	The definition of dot: The size of a defective dot over 1/2 of single pixel dot is regarded as one defective dot. Note: One pixel consists of 3 sub-pixels, including R, G, and B dot. (Sub-pixel=Dot)
Dark Dot	Dots appear dark and unchanged in size in which LCD panel is displaying pure red, green, blue pattern 	
Accidented Dot	Adjacent two sub-pixel are defect (define two dot defect)	

7.3.4.2 Inspection Standard

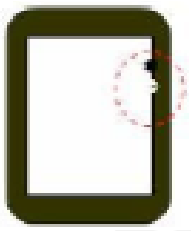
Class	Item	Criteria
Major	Bright / Dark Dot	1) LCD≤4.3"
		Bright dot: N≤0, Dark dot: N≤3, Total: N≤4
		2) 4.3"＜LCD＜7"
		Bright dot: N≤0, Dark dot: N≤4, Total: N≤6
		3) 7"≤LCD≤12"
		Bright dot: N≤4, Dark dot: N≤5, Total: N≤8
		4) LCD＞12"
		Bright dot: N≤5, Dark dot: N≤6, Total: N≤10

Class	Item	Criteria
		The distance between the two defect dots shall be greater than 5mm The distance between two defect dots above 7 inches shall be more than 10 mm **Note:** Adjacent dot defect N≤0
Minor	Spot Defects (Black spot, white spot, Pinhole, foreign matter, dent, backlight foreign matter）	Round type: as per following drawing, ∅ = (X+Y)/2 
		1) LCD≤4.3"
		D≤0.15, Ignore 0.15＜D≤0.3, N≤3 0.3＜D, N=0
		2) 4.3"＜LCD＜7"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤4 0.5＜D, N=0
		3) 7"≤LCD≤12"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤5 0.5＜D, N=0
		4) LCD＞12"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤6 0.5＜D, N=0
Minor	Bubble	1) LCD≤4.3"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤3 0.5＜D, N=0
		2) 4.3"＜LCD＜7"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤4 0.5＜D, N=0
		3) 7"≤LCD≤12"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤5 0.5＜D, N=0

Class	Item	Criteria
		4) LCD＞12"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤6 0.5＜D, N=0
Minor	Line Defect (Black/white line, backlight foreign matter)	Line type: as per following drawing 
		1) LCD≤4.3"
		W≤0.03, Ignore 0.03＜W≤0.06, L≤5, N≤3 W＞0.06, L＞5, N=0
		2) 4.3"＜LCD＜7"
		W≤0.03, Ignore 0.03＜W≤0.1, L≤5, N≤4 W＞0.1, L＞5, N=0
		3) 7"≤LCD≤12"
		W≤0.03, Ignore 0.03＜W≤0.1, L≤5, N≤5 W＞0.1, L＞5, N=0
		4) LCD＞12"
		W≤0.03, Ignore 0.03＜W≤0.1, L≤5, N≤6 W＞0.1, L＞5, N=0
Minor	Scratch	1) LCD≤4.3"
		W≤0.03, Ignore 0.03＜W≤0.2, 1.0＜L≤ 5.0, N≤3 W＞0.2, L＞5 N=0
		2) 4.3"＜LCD＜7"
		W≤0.03, Ignore 0.03＜W≤0.2, 1.0＜L≤ 5.0, N≤4 W＞0.2, L＞5, N=0
		3) 7"≤LCD≤12"
		W≤0.03, Ignore

Class	Item	Criteria	
		0.03＜W≤0.2, 1.0＜L≤ 5.0, N≤5 W＞0.2, L＞5, N=0	
		4) LCD＞12"	
		W≤0.03, Ignore 0.03＜W≤0.2, 1.0＜L≤ 5.0, N≤6 W＞0.2, L＞5, N=0	
Major	Display Abnormal	Not allowed	
Major	Outside Dimension	Accord with drawing	
Major	Glass Crack	Not allowed	
Major	Leak	Not allowed	
Minor	Corner and Side Fragment		1. Comer fragment: X, Y≤1mm Z≤T/2: allowed 2. Side fragment: X≤2.0mm Y≤1mm Z≤T/2: allowed
Major	Crack		NG
Minor	Newton's Ring (CTP or Cover Board)		Newton's ring＜1/9 area, after lightened ,no influence on words and lines

TP Standard

No.	Item	Picture	Criterion	Checking Manner	Defect Class
1	Outside dimension	-	Accord with drawing	Calipers & Eyes	Minor
2	Color deviation	Difference of ink color	Obvious deviation compared with samples	Eyes	Minor
3	Ink pinhole		No any holes near VA side 3mm Out of VA: D≤0.15mm N≤1, no present in reflection condition.	Eyes Film	Minor
4	Ink saw tooth		W≤0.15mm N=1	Eyes Film	Minor
5	Ink light leakage		1. width of light leakage at the edge area ≤0.15mm OK 2. width of light leakage at the edge area >0.15mm NG	Eyes Film	Minor
6	Cover glass profile	-	No ink, adhesive, oil stain, etc	Eyes	Minor
7	IR(LED)dot/black white dot		φ≤0.2、N≤1 0.15< φ 、not allowed	Eyes& Film	MIN
8	IR(LED)dot black white dot/different color		no present when use all viewing angle to determine at 35cm, allowed	Eyes	MIN
9	Shooting hole		φ≤0.2、N≤1 0.15< φ 、not allowed	Eyes& Film	MIN

7.4 Dealing with Customer Complaints

7.4.1 Non-conforming Analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.

After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.4.2 Handling of Non-conforming Displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8. Reliability Specification

8.1 Reliability Tests

Item	Test Condition	
High Temperature Storage	80±2℃/240 hours	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Sealleak; 3.Non-display; 4.Missing segments; 5.Glass crack; 6.Current Idd is twice higher than initial value.
Low Temperature Storage	-30±2℃/240 hours	
High Temperature Operating	70±2℃/240 hours	
Low Temperature Operating	-20±2℃/240 hours	
Temperature Cycle	-30℃~ 25℃~80℃ × 10cycles (30min.) (5min.) (30min.)	
Vibration Test	40℃±5℃×90%RH/96 hours	
Damp Proof Test	Frequency：10Hz~55Hz~10Hz Amplitude: 1.5mm, X, Y, Z direction for total 3hours (Packing condition)	
Vibration Test	Drop to the ground from 1m height, one time, every side of carton. (Packing condition)	
Dropping Test	Voltage: ±8KV R: 330Ω C: 150pF Air discharge, 10time	
ESD Test	Voltage: ±6KV R: 330Ω C: 150pF Contact discharge, 10time	

Note 1: The test samples should be applied to only one test item.
Note 2: Sample size for each test item is 5~10pcs.
Note 3: For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.
Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
Note 5: Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
Note 6: Please use automatic switch menu (or roll menu) testing mode when test operating mode.

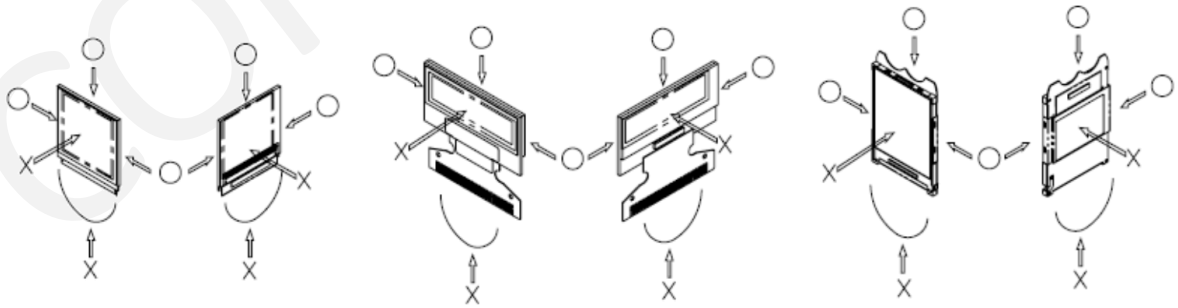
8.1.1 Inspection Check Standard

After the completion of the described reliability test, the samples are to be left at room temperature for 4 hrs prior to conducting the inspection check at 25±5 °C, 65±5% RH.

9. Handling Precautions

9.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water
4) If pressure is applied to the display surface or its neighbourhood of the display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
5) The polarizer covering the surface of the display module is soft and easily scratched. Please be careful when handling the display module.
6) When the surface of the polarizer of the display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   a. Scotch Mending Tape No. 810 or an equivalent
   b. Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   c. Also, pay attention that the following liquid and solvent may spoil the polarizer:
      - Water
      - Ketone
      - Aromatic Solvents
7) Hold the display module very carefully when placing it into the system housing. Do not apply excessive stress or pressure to display module. And, do not over bend the film with electrode pattern layouts. These stresses will



influence the display performance. Also, secure sufficient rigidity for the outer cases.
8) Do not apply stress to the LSI chips and the surrounding molded sections.
9) Do not disassemble nor modify the display module.
10) Do not apply input signals while the logic power is off.
11) Pay sufficient attention to the working environments when handing display modules to prevent occurrence of element breakage accidents by static electricity.

a. Be sure to make human body grounding when handling display modules.
b. Be sure to ground tools to use or assembly such as soldering irons.
c. To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
d. Protective film is being applied to the surface of the display panel of the display module. Be careful since static electricity may be generated when exfoliating the protective film.

12) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. If the display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
13) If electric current is applied when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 Storage Precautions

1) When storing display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the display module, when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the display module, fasten the external plastic housing section.
7) If power supply to the display module is forcibly shut down by such errors as taking out the main battery while the display panel is in operation, we cannot guarantee the quality of this display module.

9.4 Operation Precautions

1) It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.
2) Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation.
3) Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged.
4) To protect display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the display modules.
   a. Pins and electrodes
   b. Pattern layouts such as the FPC
5) When the driver is being exposed (COG), semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if the driver is exposed to light, malfunctioning may occur.
   a. Design the product and installation method so that the driver may be shielded from light in actual usage.
   b. Design the product and installation method so that the driver may be shielded from light during the inspection processes.
6) Although the display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
7) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

9.5 Other Precautions

1) Request the qualified companies to handle industrial wastes when disposing of the display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.