DMT050WVNMCMI-1H

PRODUCT SPECIFICATION

Version 0.1
Aug 16, 2023

TBD

Customer's Approval	
Signature	*Date*

Prepared by *Yvette Hsieh*
Approved by *Evan Huang*

Revision History

VERSION	DATE	DESCRIPTION	AUTHOR
0.1	Aug 16, 2023	Preliminary	Yvette Hsieh

Legal Notice

Table of Contents

1. General Description

1.1 Introduction

This is n 5.0” size colour active matrix TFT LCD module that uses amorphous silicon TFT as a switching device. The display is normally black mode, transmissive, and featuring high contrast and excellent colour saturation. The resolution of the TFT-LCD is 480 x 854 and can display up to 16.7M colours. The display module supports 2-Lane MIPI interface and optical bonding touch panel.

1.2 Main Features

Item	Contents
Display Type	TFT LCD
Screen Size	5.0” Diagonal
Display Format	480 x RGB x 854 Dots
No. of Colour	65K/262K/16.7M
Overall Dimensions	67.26 (W) x 122.00 (H) x 3.98 (D) mm
Active Area	61.6320 (W) x 109.6536 (H) mm
Mode	Normally black / Transmissive
Surface Treatment	Glare (6H)
Viewing Direction	All round
Interface	2-Lane MIPI
Driver IC	ILI9806E
Backlight Type	LED, White, 12 chips
Touch Panel	PCT
Touch Interface	I^2C
Touch Driver IC	GT911
Bonding Type	Optical Bonding
Operating Temperature	-20°C ~ 70°C
Storage Temperature	-30°C ~ 80°C
ROHS	Compliant to RoHS

1.3 CTP Features

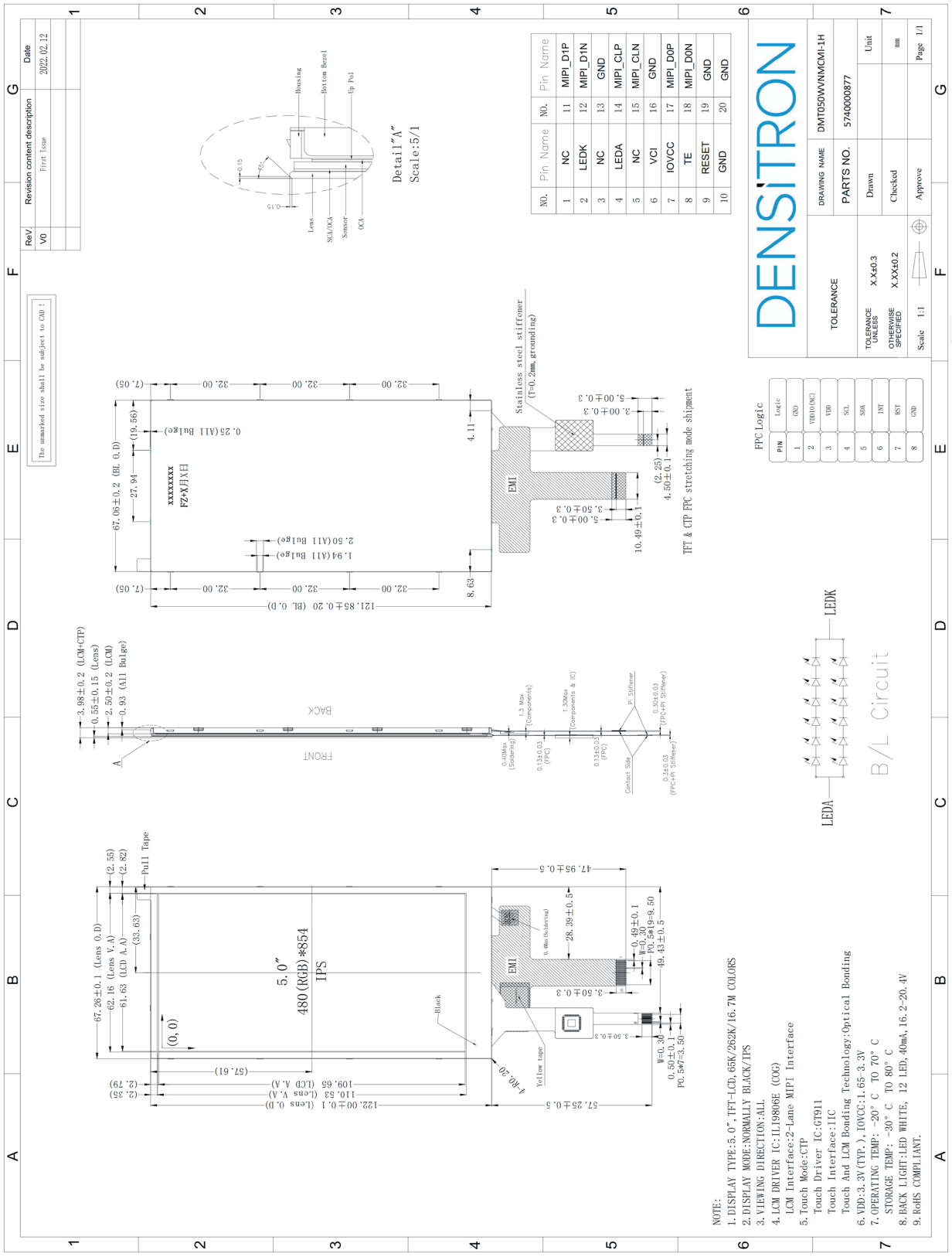
Item	Contents
Touch Panel	PCT
Structure	G+G
Controller IC	GT911
Interface	I^2C
Slave Address	0x5D(7bit) or 0x14(7bit)
Touch Mode	Five fingers
Logic Level	3.3V

2. Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Display Format	480 x RGB x 854	Dots
Overall Dimensions	67.26 (W) x 122.00 (H) x 3.98 (D)	mm
Active Area	61.6320 (W) x 109.6536 (H)	mm
Dot Pitch	0.1284 x 0.1284 (H)	mm
Weight	TBD	g
IC Controller/Driver	ILI9806E	

2.2 Mechanical Drawing



3. Electrical Specification

3.1 Absolute Maximum Ratings

(Ta=25°C, VSS=0)

Item	Symbol	Min	Max	Unit
Digital Supply Voltage	V_{CI}	-0.3	6.5	V
Digital Interface Supply Voltage	I_{OVCC}	-0.3	3.3	V
Operating Temperature	T_{OP}	-20	+72	°C
Storage Temperature	T_{ST}	-30	+80	°C

Note 1: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. For normal operations, it is desirable to use this module under the conditions according to Section 3.2 “Electrical Characteristics”, to avoid malfunctioning.

Note 2: Please refer to item of RELIABILITY.

3.2 Electrical Characteristics

3.2.1 DC Electrical Characteristics

Item	Symbol	Min	Typ.	Max	Unit
Digital Supply Voltage	V_{CI}	2.5	3.3	6.0	V
Digital Interface Supply Voltage	I_{OVCC}	1.65	1.8	3.3	V
Normal Mode Current Consumption	I_{DD}	-	40	80	mA
Level Input Voltage	V_{IH}	0.7 I_{OVCC}	-	I_{OVCC}	V
	V_{IL}	-0.3	-	0.3 I_{OVCC}	V
Level Output Voltage	V_{OH}	0.8 I_{OVCC}	-	I_{OVCC}	V
	V_{OL}	GND	-	0.2 I_{OVCC}	V

3.3 Interface Pin Assignment

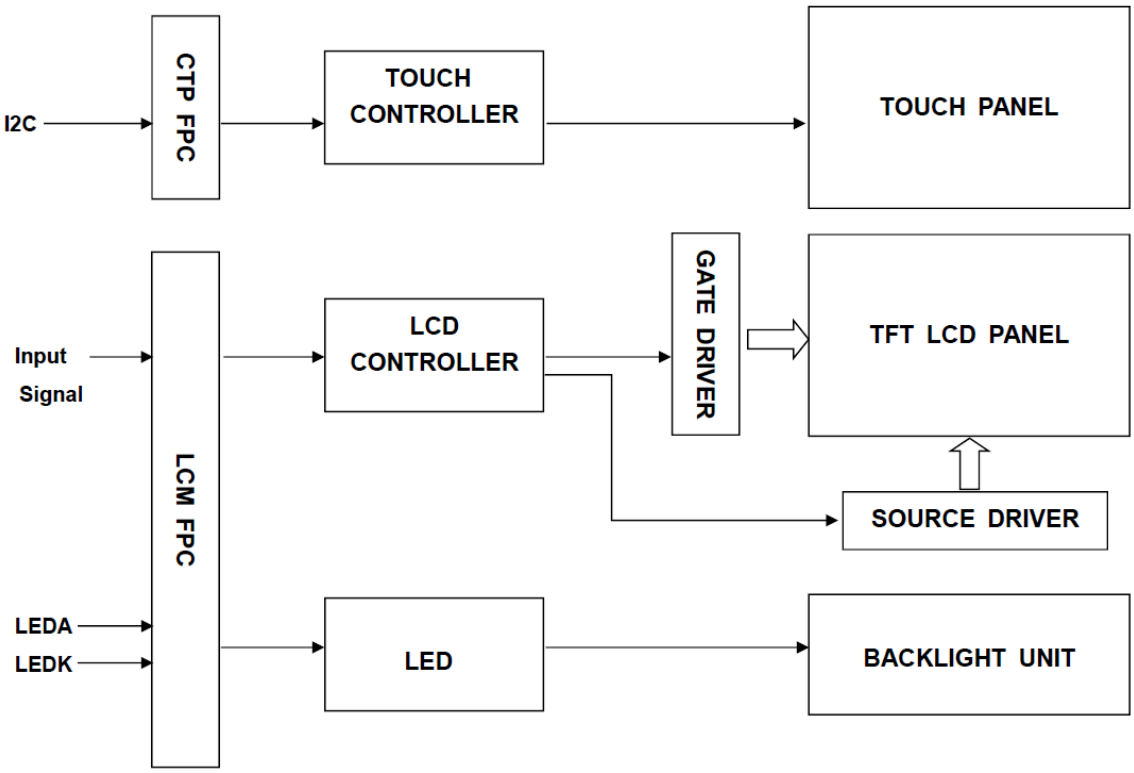
3.3.1 TFT Pin Definition

No.	Symbol	I/O	Function
1	NC-	-	-
2	LDEK	P	Cathode pin of backlight
3	NC	-	-
4	LEDA	P	Anode pin of backlight
5	NC	-	-
6	VCI	P	Supply voltage (3.3V)
7	IOVCC	P	I/O power supply voltage
8	TE	O	Tearing effect output. Leave the pin to open when not in use.
9	RESET	I	The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
10	GND	P	Ground
11	MIPI_D1P	I/O	MIPI DSI differential data pair (DSI-Dn +/-). If MIPI are not used, they should be connected to DGND.
12	MIPI_D1N	I/O	
13	GND	P	Ground
14	MIPI_CLP	I	MIPI DSI differential clock pair (DSI-CLK +/-). If MIPI are not used, they should be connected to DGND.
15	MIPI_CLN	I	
16	GND	P	Ground
17	MIPI_D0P	I/O	MIPI DSI differential data pair (DSI-Dn +/-). If MIPI are not used, they should be connected to DGND.
18	MIPI_D0N	I/O	
19-20	GND	P	Ground

3.3.2 CTP Interface Description

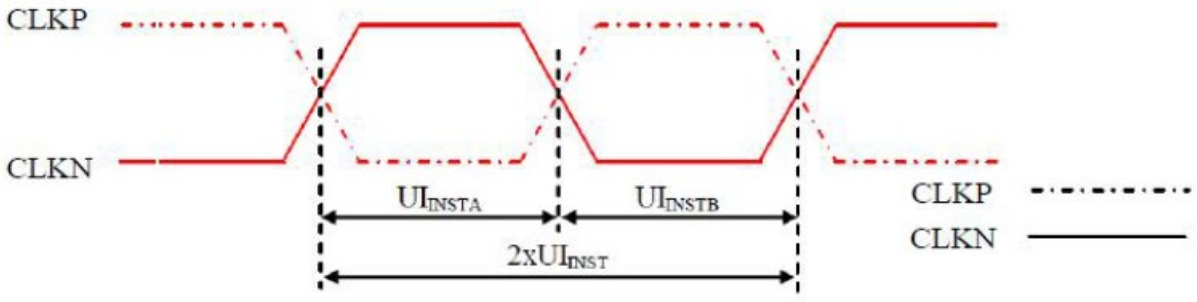
No.	Symbol	I/O	Function
1	GND	P	Ground
2	VDDIO (NC)	-	No connection
3	VDD	P	Supply voltage
4	SCL	I	I^2C clock input
5	SDA	I	I^2C data input and out put
6	INT	I	External interrupt to the host
7	RST	I	External reset, low is active
8	GND	P	Ground

3.4 Block Diagram



3.5 Timing Characteristics

3.5.1 High Speed Mode – Clock Channel Timing



DSI Clock Channel Timing

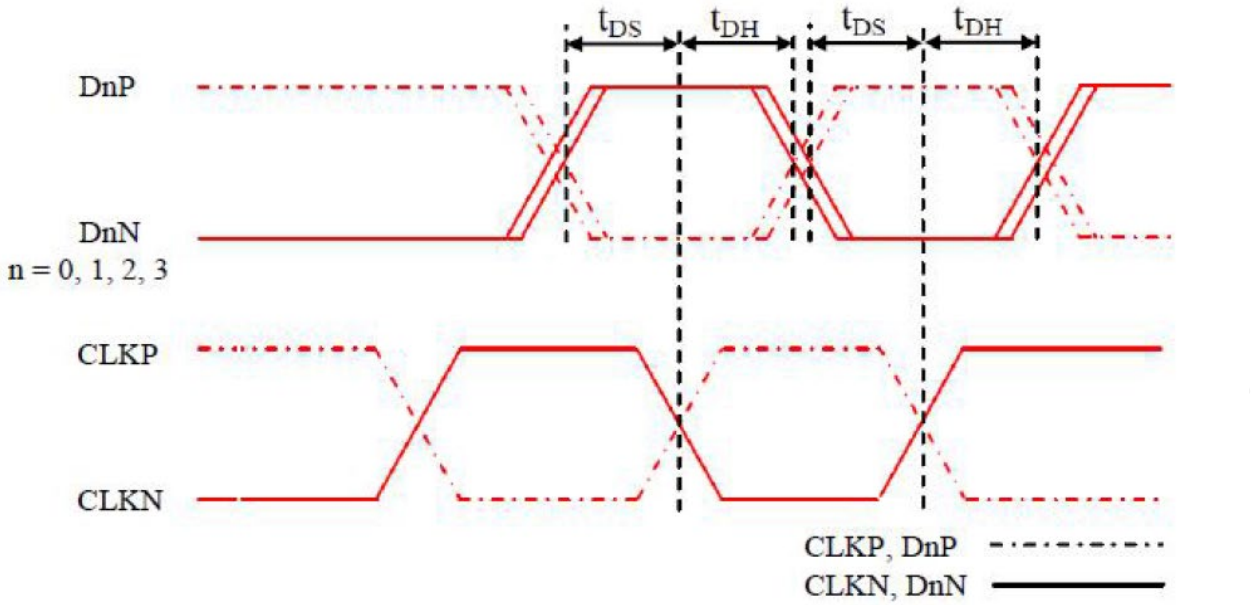
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INISTB}	UI instantaneous	2	12.5	ns

Note 1: UI = UI_{INSTA} = UI_{INISTB}

Note 2: Define the minimum value of 24 UI per pixel please see below

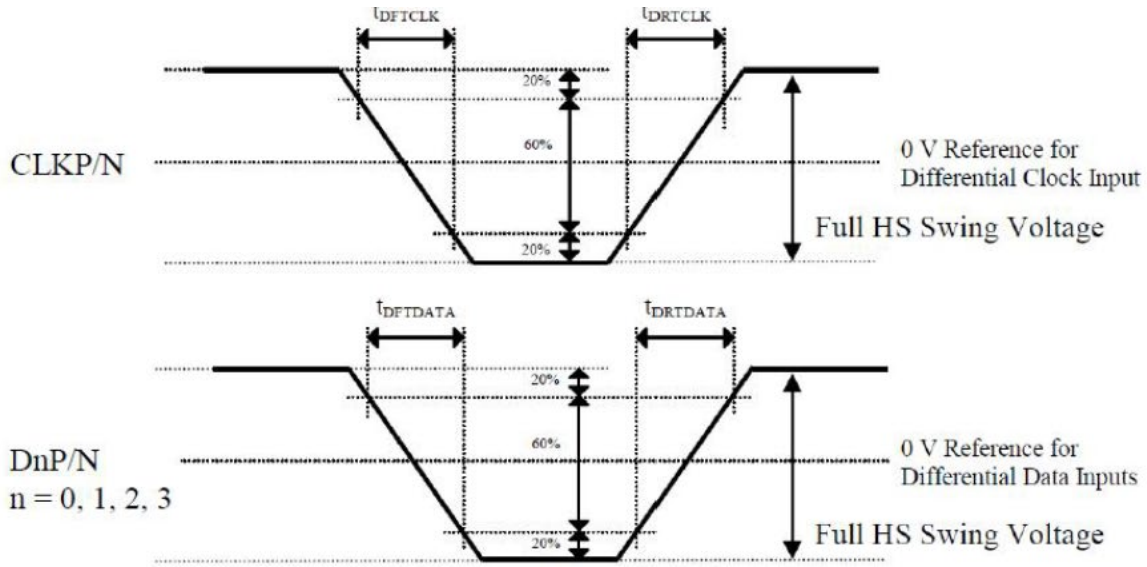
Data Type	Two Lanes Speed	Three Lanes Speed	Four Lanes Speed
Data type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data type = 10 1110 (2Eh), RGB 666 loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

3.5.2 High Speed Mode – Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max
DnP/N, n = 0 and 1	t_{DS}	Data to clock setup time	0.15xUI	-
	t_{DH}	Clock to data setup time	0.15xUI	-

3.5.3 High Speed Mode – Rising and Fall Timing

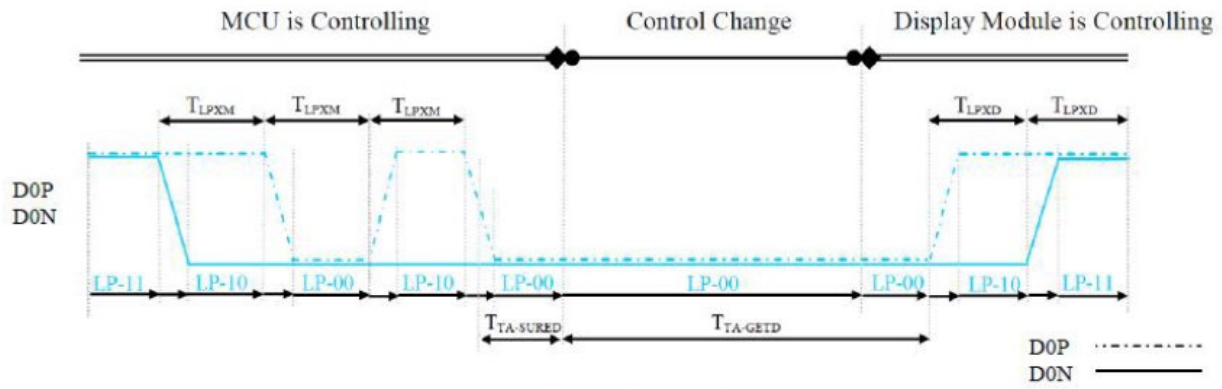


Parameter	Symbol	Condition	Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n = 0 and 1	150 ps	-	0.3UI
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n = 0 and 1	150 ps	-	0.3UI

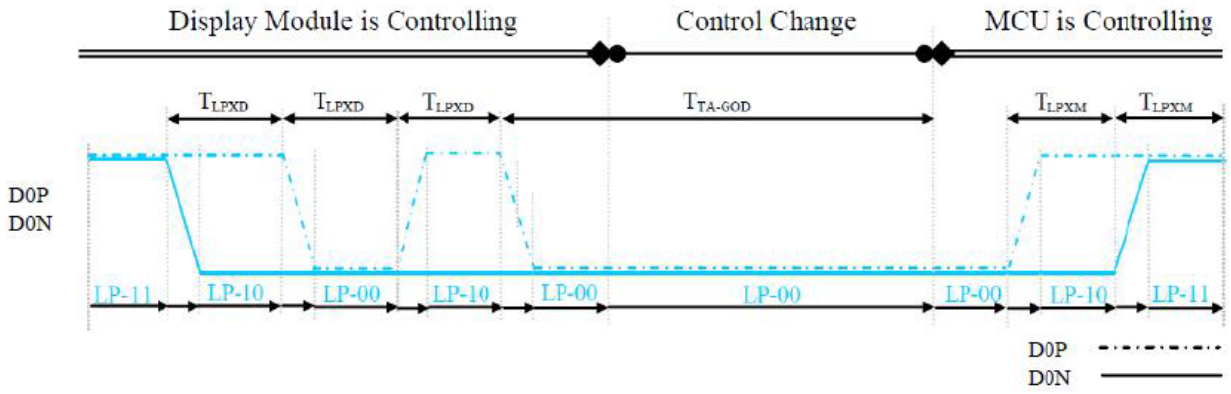
Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

3.5.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bys Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.



Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.



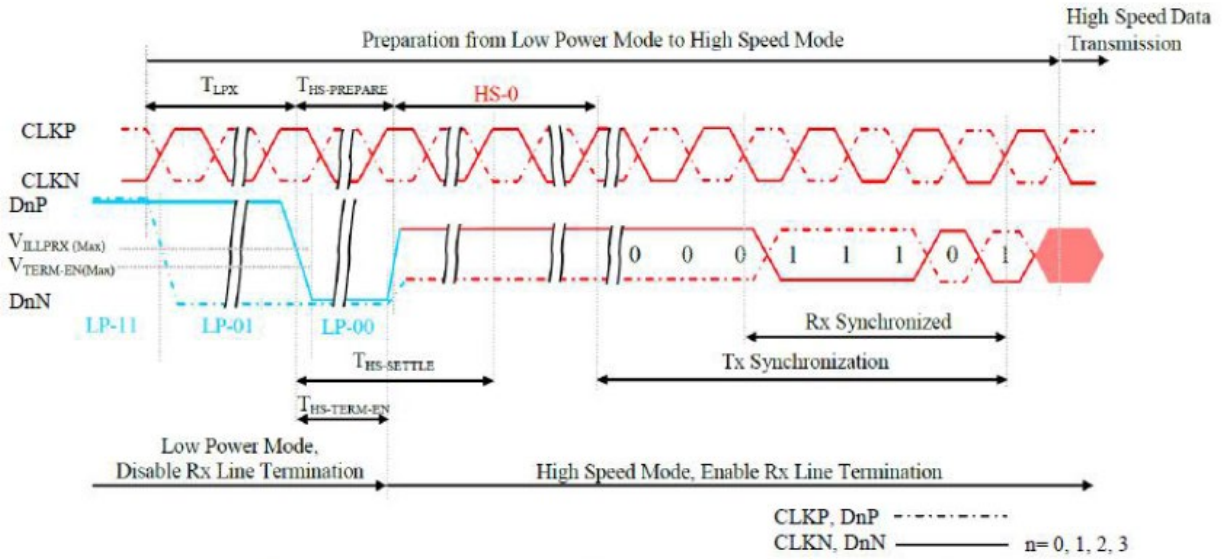
Low Power State Period Timings - A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-10 or LP-11 periods. MCU→Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-10 or LP-11 periods. Display Module (ILI9881C) →MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	TLPXD	2xTLPXD	ns

Low Power State Period Timings – B

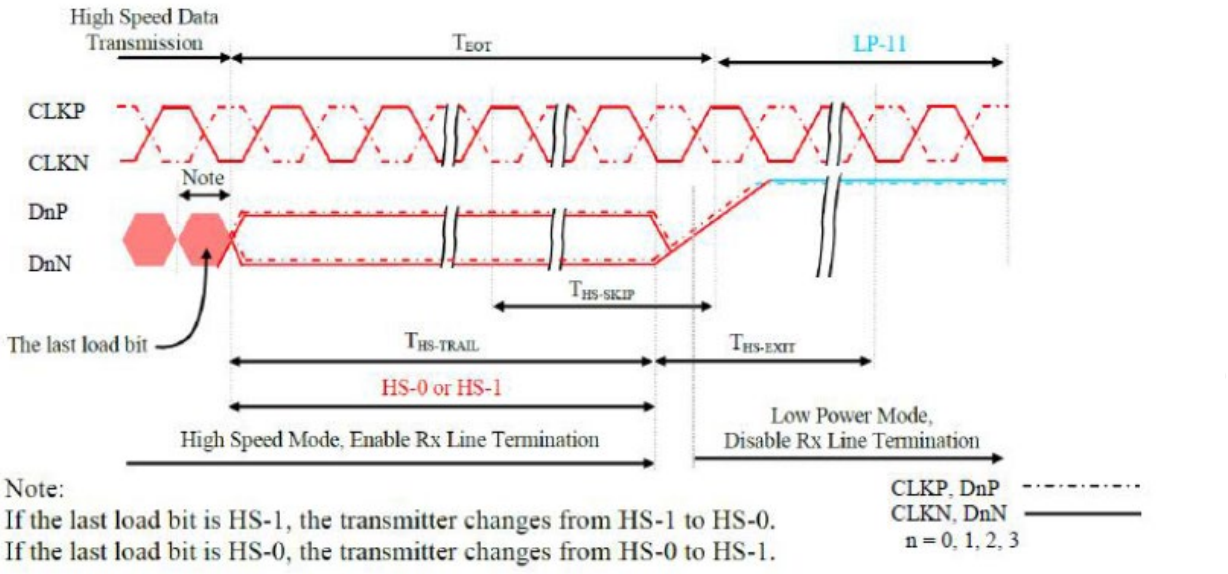
Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GATED}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MCU	$4xT_{LPXD}$	ns

3.5.5 Low Speed Mode – Bus Turn Around



Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

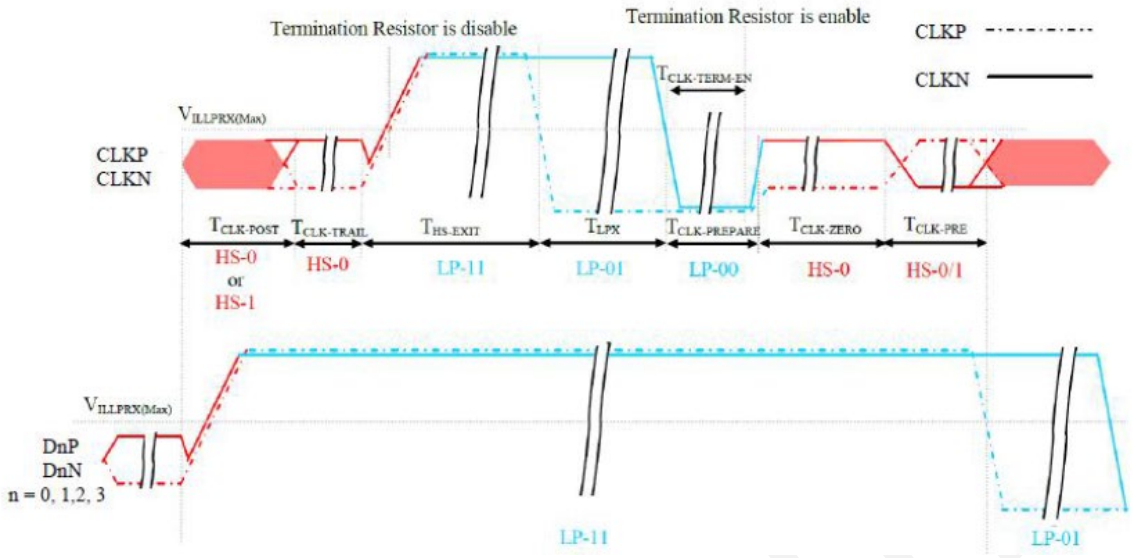
3.5.6 Data Lanes from High Power Mode to High Speed Mode



Data Lanes – High Speed Mode to Low Power Mode Timing

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time driver LP-11 after HS burst	100	-	ns

3.5.7 SCI Clock Burst – High Speed Mode to/from Low Power Mode

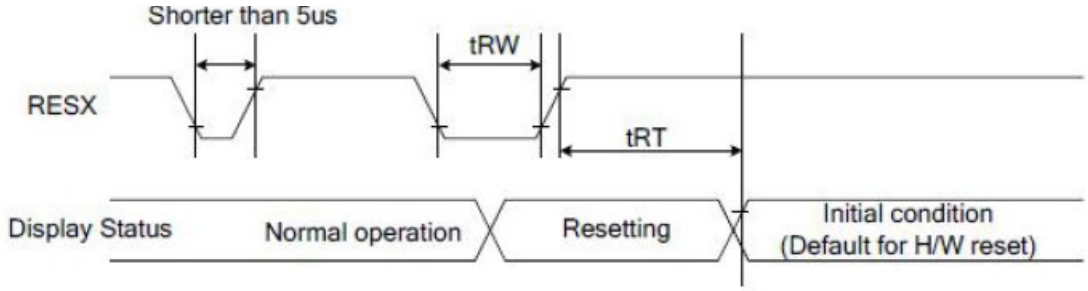


Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PERPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CKL-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

3.5.8 Timing for DSI Video Mode

Parameter	Symbol	Min	Typ	Max	Unit
DCLK Frequency	FCLK	-	29	-	MHz
Horizontal Display Area	HDSIP	-	480	-	Clock
Horizontal Sync Width	hpw	1	4	-	Clock
Horizontal Sync Back Porch	hbp	1	30	-	Clock
Horizontal Sync Front Porch	hfp	1	18	-	Clock
Vertical Display Area	VDISP	-	854	-	Line
Vertical Sync Width	vs	1	4	-	Line
Vertical Sync Back Porch	vbp	1	30	-	Line
Vertical Sync Front Porch	vfp	1	20	-	Line
Frame-Rate	-	-	60	-	Hz

3.5.9 Reset Input Timing



Signal	Symbol	Parameter	Min	Max	Unit	Note
RESX	t_{RW}	Reset pulse duration	10	-	us	-
	t_{RT}	Reset cancel	-	5	ms	1, 5
			-	120	ms	1, 6, 7

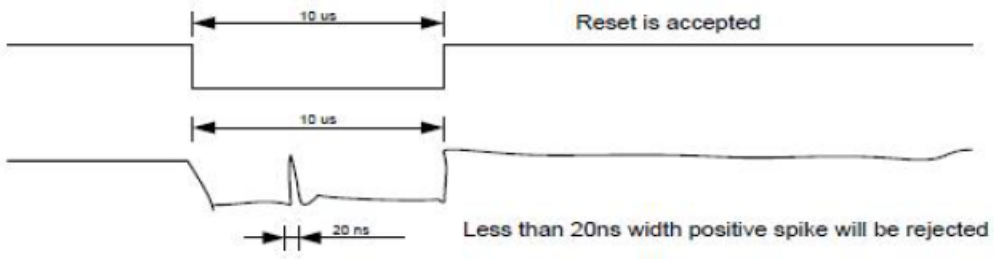
Note 1: The reset cancel also includes require time for loading ID Bytes, VCOM setting and other setting from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (the display enter the blanking sequence, which maximum time is 120ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection can also be applied during a valid reset pulse, as shown below.



Note 5: When Reset applied during Sleep In mode.

Note 6: When Reset applied during Sleep Out mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

4. Electrical Specification Touch

4.1 Electrical Characteristics

4.1.1 Absolute Maximum Rating

Item	Symbol	Min	Max	Unit
Power Supply Voltage	V_{DD}	2.66	3.47	V
Operating Temperature	T_{OP}	-20	+70	˚C
Storage Temperature	T_{ST}	-30	+80	˚C

4.1.2 DC Electrical Characteristics

(Ta=25˚C, VDD=2.8V, VDDIO=1.8V or VDDIO=VDD)

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD	2.66	3.3	3.47	V
Normal Mode Operating Cueernt	-	-	8	14.5	mA
Green Mode Operating Cueernt	-	-	3.3	-	mA
Sleep Mode Operating Cueernt		70	-	120	uA
Doze Mode Operating Cueernt		-	0.78	-	mA
Digital Input Low Voltage	V_{IL}	-0.3	-	0.25 VDD	V
Digital Input High Voltage	V_{IH}	0.75 VDD	-	VDD +0.3	V
Digital Output Low Voltage	V_{OL}	-	-	0.15VDD	V
Digital Output High Voltage	V_{OH}	0.85 VDD	-	-	V

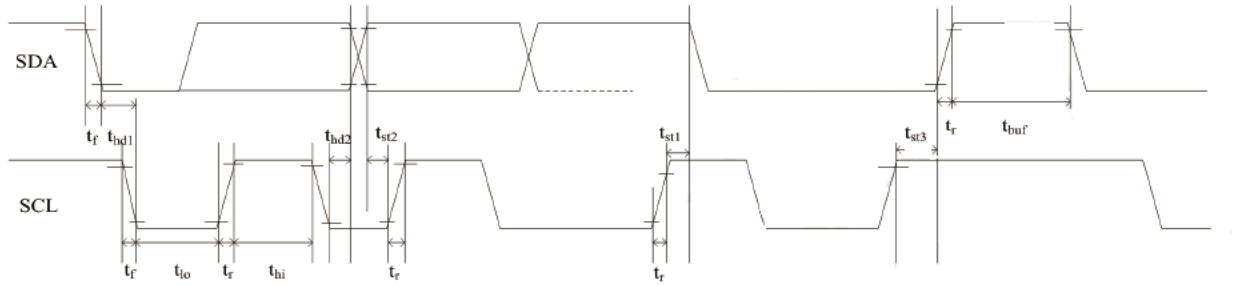
4.1.3 AC Characteristics

(Ta=25˚C, VDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit
OSC Oscillation Frequency	59	60	61	MHz
I/O Output Rise Time, Low to High	-	14	-	ns
I/O Output Fall Time, High to Low	-	14	-	ns

4.2 I²C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I²C timing is shown below.



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor.

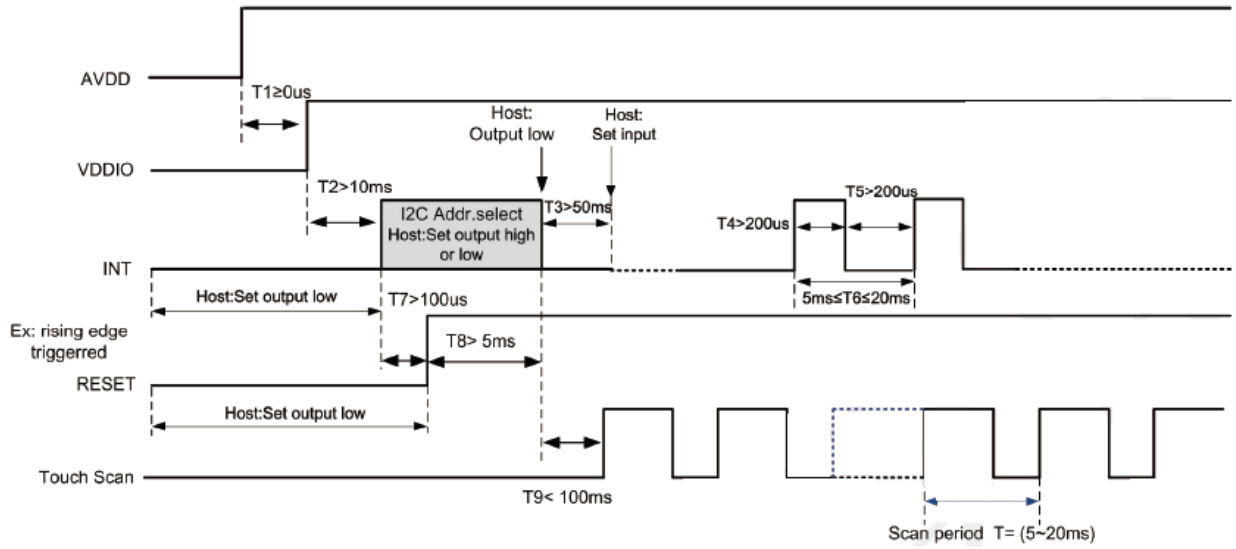
Parameter	Symbol	Min	Max	Unit
SCL Low Period	T_{lo}	1.3	-	us
SCL High Period	t_{hi}	0.6	-	us
SCL Setup time for Start Condition	t_{st1}	0.6	-	us
SCL Setup Time for Stop Condition	t_{st3}	0.6	-	us
SCL Hold Time for Start Condition	t_{hd1}	0.6	-	us
SDA Setup Time	t_{st2}	0.1	-	us
SDA Hold Time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor.

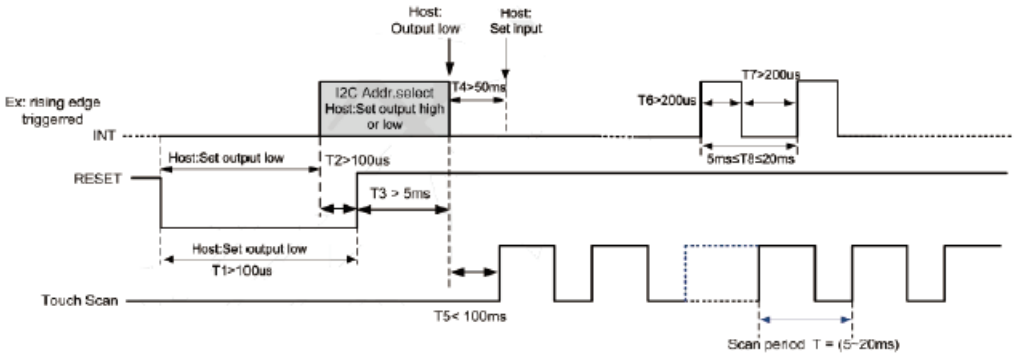
Parameter	Symbol	Min	Max	Unit
SCL Low Period	Tl_o	1.3	-	us
SCL High Period	t_{hi}	0.6	-	us
SCL Setup time for Start Condition	t_{st1}	0.6	-	us
SCL Setup Time for Stop Condition	t_{st3}	0.6	-	us
SCL Hold Time for Start Condition	t_{hd1}	0.6	-	us
SDA Setup Time	t_{st2}	0.1	-	us
SDA Hold Time	t_{hd2}	0	-	us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings.

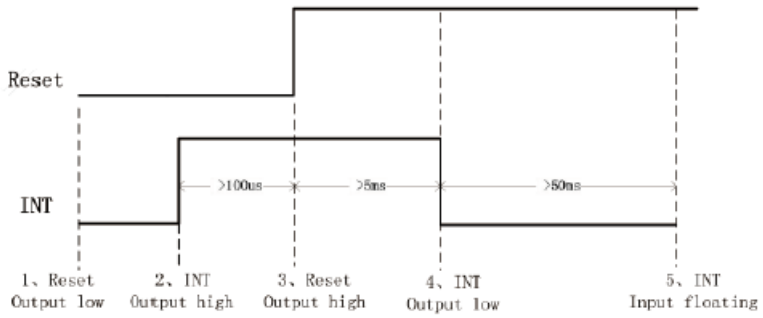
Power-on Timing



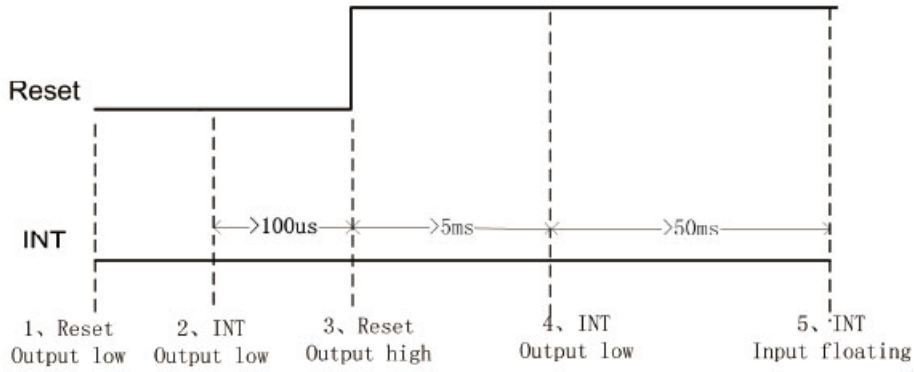
Time for host resetting GT911



Time for setting address to 0x28/0x29



Timing for setting slave address to 0xBA/0xBB



a) Data Transmission

(For example, device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

All slave devices connected to I^2C bus should detect the 8-bit address issued after Start condition and send to correct ACL. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0xBA or 0xBB, GT91 will stay in an idle state.

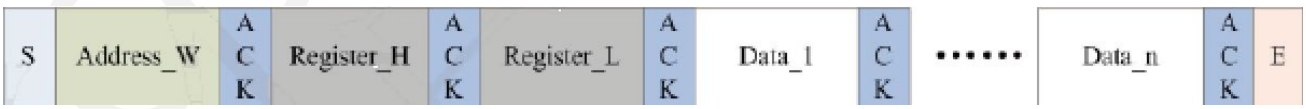
For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data bytes consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example, device address is 0xBA/0xBB)

Timing for Write Operation



The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0xBA (address hits and R/W bit, R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example, device address is 0xBA/0xBB)

Timing for Read Operation

The diagram above displays the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0xBA (address hits and R/W bit, R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0xBB (Read Operating). After ACK, the host start to read data.

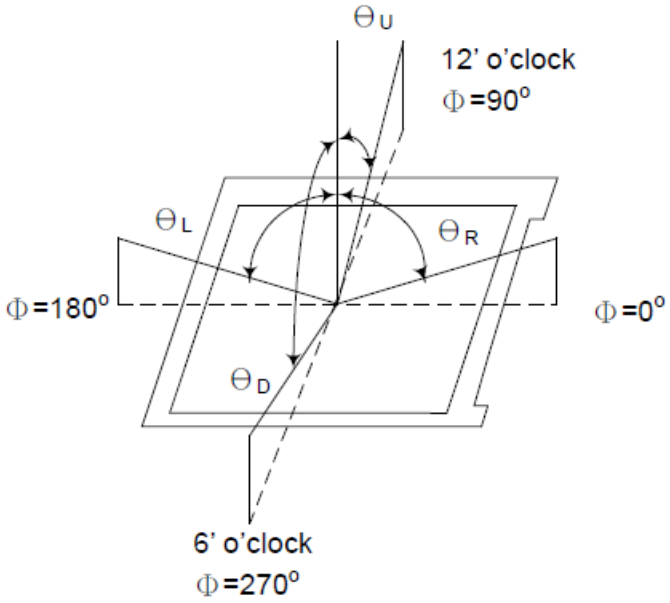
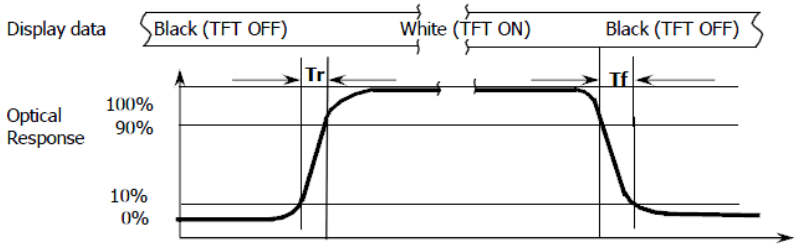
GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

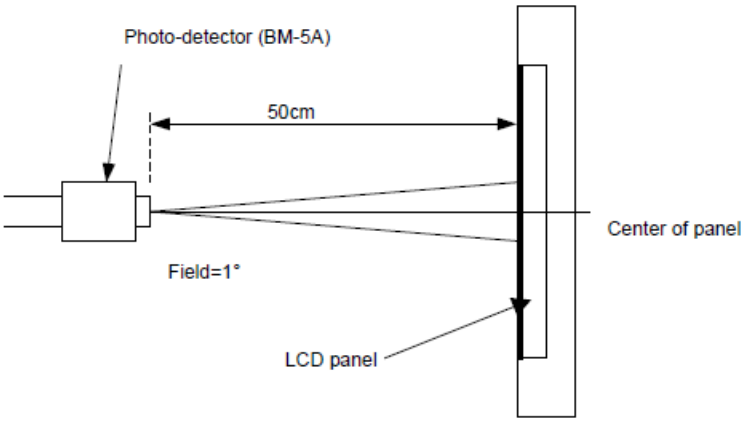
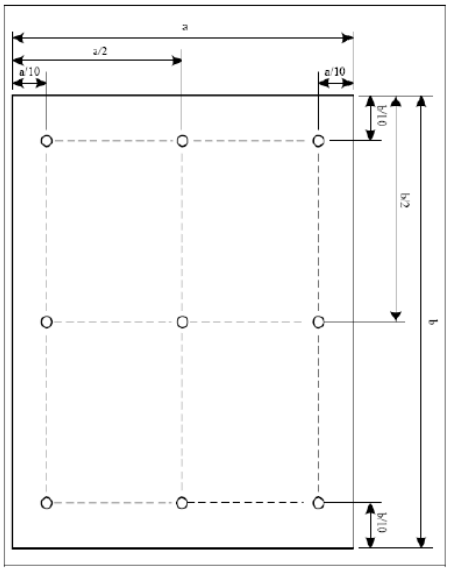
5. Optical Specification

5.1 Optical Characteristics

Characteristics		Symbol	Conditions	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	θ = 0° Normal viewing angle	600	1000	-	-	1, 2
Response time		$T_R + T_F$		-	16	21	msec	1, 3
Color Gamut		S(%)	-	-	62	-	%	-
Viewing Angle	Left	θ_L	CR≧10	-	80	-	-	1, 4
	Right	θ_R		-	80	-		
	Up	θ_U		-	80	-		
	Down	θ_D		-	80	-		
Colour Chromaticity	Red	Rx	θ = 0° Normal viewing angle	0.602	0.642	0.682	-	1, 4 CA-310
		Ry		0.306	0.346	0.386		
	Green	Gx		0.280	0.320	0.360		
		Gy		0.576	0.616	0.656		
	Blue	Bx		0.102	0.142	0.182		
		By		0.039	0.079	0.119		
	White	Wx		0.250	0.290	0.330		
		Wy		0.282	0.322	0.362		
Luminance		Lv	-	310	360	-	cd/m^2	5
Uniformity		Avg	-	80	-	-	%	5

Note: Measuring Condition = in dark room, at ambient temperature 25±2°C, for 15min. warm-up time.

Note	Item	Test method
1	Definition of Viewing Angle	
2	Definition of Contrast Ratio (CR)	measured at the center point of panel $CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$
3	Definition of Response Time	

Note	Item	Test method
4	Definition of optical measurement setup	
5	Definition of Luminance Uniformity	Luminance Uniformity of these 9 points is defined as below  $\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$

6. LED Backlight Specification

6.1 LED Backlight Characteristics

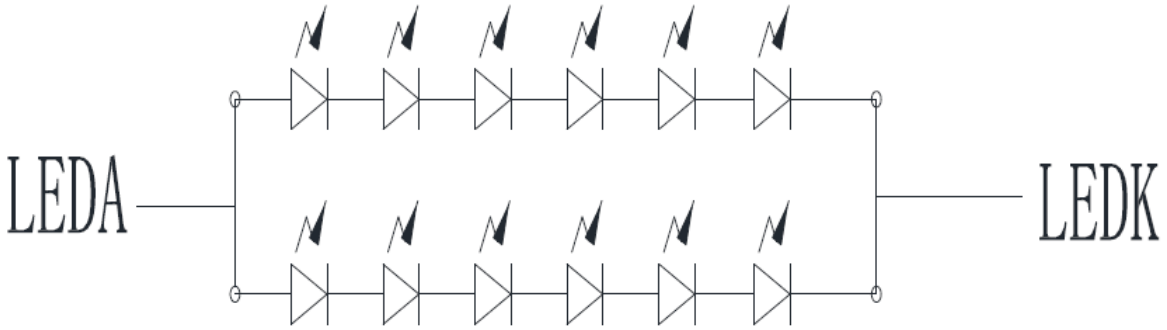
The back-light system is edge-lighting type with 12 chips LED.

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	I_F	30	40	-	mA	-
Forward Voltage	V_F	-	19.2	-	V	-
LED Lifetime	Hr	50000	-	-	Hrs	1, 2

Note 1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta = 25±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

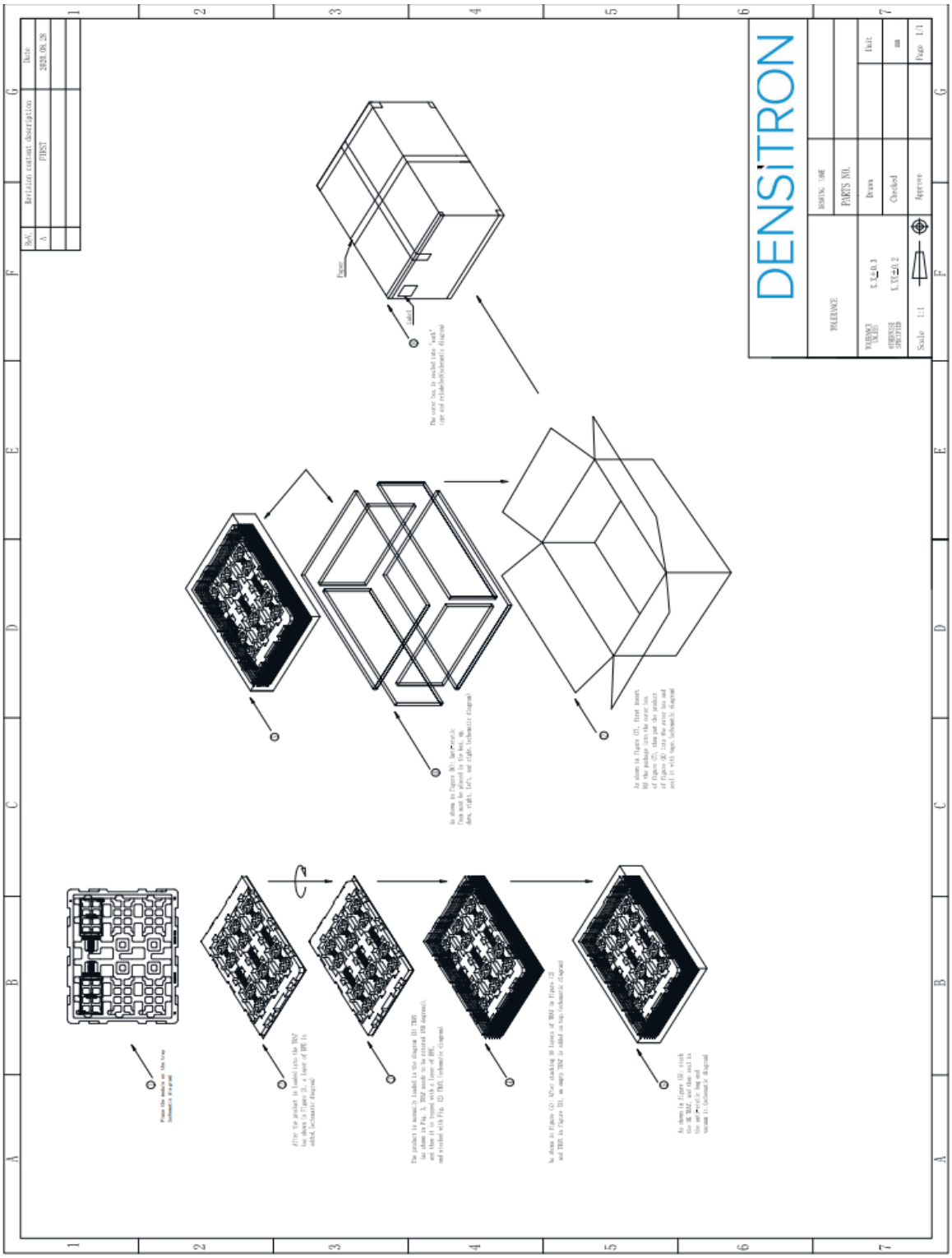
Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta = 25°C and IL = 40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.

6.2 Internal Circuit Diagram



CIRCUIT DIAGRAM

7. Packaging


DENSITRON
PARTS NO.
Drawn
Checked
Approve
Scale 1:1
Unit
Page 1/1

8. Quality Assurance Specification

8.1 Conformity

The performance, function and reliability of the shipped products conform to the Product Specification.

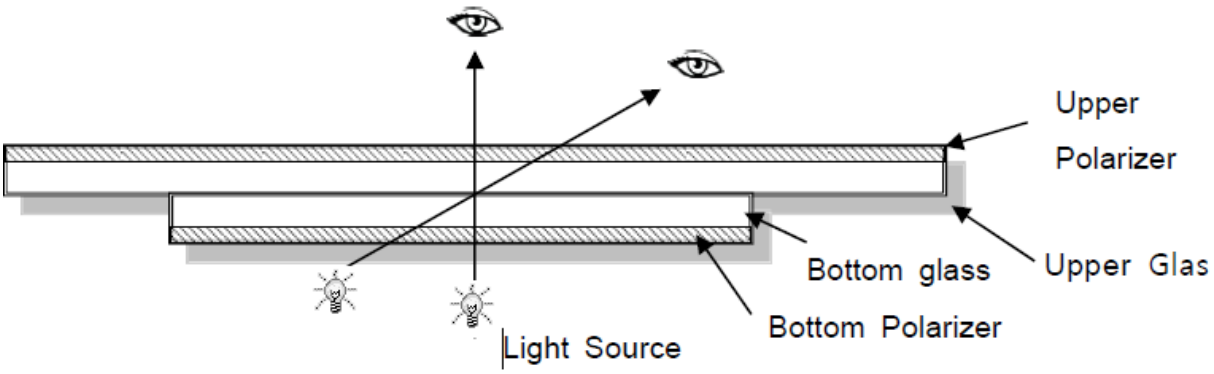
8.2 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	25 ± 5°C
Humidity:	65% ± 10% RH
Viewing Angle:	Normal viewing angle
Illumination:	300 to 700 Lux (Single fluorescent lamp)
Viewing distance:	30 to 50cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.



8.3 Delivery Assurance

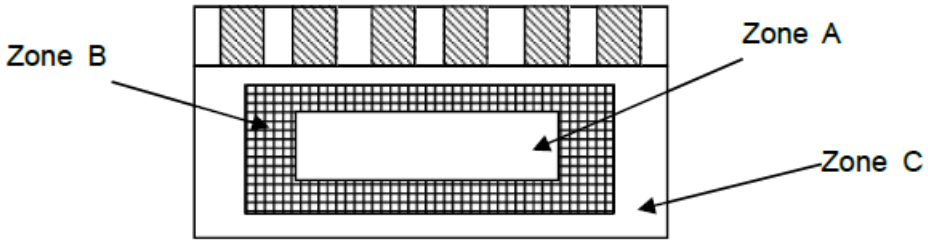
8.3.1 Delivery Inspection Standards

Class II, Normal Inspection, ISO2859-1

8.3.2 Criteria & Acceptable Quality Level

Classification of defects	AQL
Major	0.65
Minor	1.5

8.3.3 Zone Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A+Zone B) which cannot be seen after assembly by customer.)

Note: As a general rule, visual defects in Zone C can be ignored when it doesn't affect product function or appearance after assembly by customer.

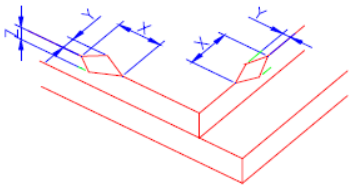
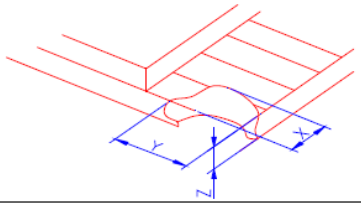
8.3.4 Criteria & Classification

No	Items	Criteria	Classification of defects
1	Functional Defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting ect	Major
2	Missing	Missing components and ect	
3	Outline Dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color Tone	Color unevenness refer to limited sample	Minor
5	Spot/Line Defect	Light dot, Dim spot, Polarizer Air Bubble, Polarizer accidented spot and etc	
6	Soldering Appearance	Good soldering, Peeling off is not allowed and etc	
7	LDC/Polarizer/CTP	Black/White spot/line, scratch, crack etc	

Note1: a) Light dot Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

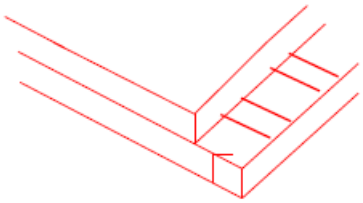
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

Criteria (Visual)

<table>
<tr><th>Number</th><th>Criteria (mm)</th></tr>
<tr><td rowspan="2">1.0 LCD Crack/Broken
X: Length, Y: Width, Z: Height
L: Length of ITO, T: Height of LCD</td><td>The edge of LCD broken
 
<table>
<tr><th>X</th><th>Y</th><th>X</th></tr>
<tr><td>≤ 3.0</td><td>< Inner border line of the seal</td><td>≤ T</td></tr>
</table></td></tr>
<tr><td>LDC corner broken
 
<table>
<tr><th>X</th><th>Y</th><th>X</th></tr>
</table></td></tr>
</table>

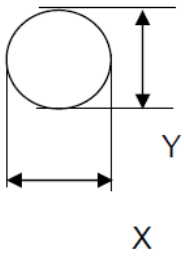
	≤ 3.0	≤ L	≤ T

LCD crack



Crack not allowed

2.0 Spot Defect



Φ=(X+Y)/2

1. Light dot (black/white spot, pinhole, stain etc.

Size/Zone	Acceptable Qty		
	A	B	C
Φ ≤ 0.15	Ignore	Ignore	
0.15 < Φ ≤ 0.25	3 (distance ≥ 10mm)		
0.25 < Φ ≤ 0.4	2 (distance ≥ 10mm		
Φ > 0.4	0		

2. Dim spot (light leakage, dent, dark spot etc.

Size/Zone	Acceptable Qty		
	A	B	C
Φ ≤ 0.15	Ignore	Ignore	
0.15 < Φ ≤ 0.25	3 (distance ≥ 10mm)		
0.25 < Φ ≤ 0.4	2 (distance ≥ 10mm		
Φ > 0.4	0		

3. Polarizer accidented spot

Size/Zone	Acceptable Qty		
	A	B	C
Φ ≤ 0.2	Ignore	Ignore	
0.2 < Φ ≤ 0.5	2 (distance ≥ 10mm)		
Φ > 0.5	0		

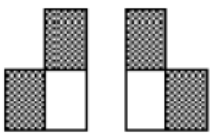
4. Polarizer bubble

Size/Zone	Acceptable Qty		
	A	B	C
Φ ≤ 0.2	Ignore	Ignore	

<table>
<tr><td></td><td>
<table>
<tr><td>0.2 < Φ ≤ 0.4</td><td>2 (distance ≥ 10mm)</td><td rowspan="2"></td></tr>
<tr><td>Φ > 0.4</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>3.0 LCD Pixel defect</td><td>
Pixel bad points
<table>
<tr><th>Item</th><th>Zone A</th><th>Acceptable Qty</th></tr>
<tr><td rowspan="3">Bright dot</td><td>Radom</td><td>N ≤ 2</td></tr>
<tr><td>2 dots adjacent</td><td>N ≤ 0</td></tr>
<tr><td>3 dots adjacent</td><td>N ≤ 0</td></tr>
<tr><td rowspan="3">Dark dot</td><td>Radom</td><td>N ≤ 3</td></tr>
<tr><td>2 dots adjacent</td><td>N ≤ 0</td></tr>
<tr><td>3 dots adjacent</td><td>N ≤ 0</td></tr>
<tr><td>Distance</td><td>1. Minimum distance between bright dots
2. Minimum distance between dark dots
3. Minimum distance between dark and bright dots</td><td>5mm</td></tr>
<tr><td colspan="2">Total bright and dark dots</td><td>N ≤ 4</td></tr>
</table>
Note 1: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
Note 2: Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.
Note 3: 2 dot adjacent = 1 pair = 2 dots

2 dot adjacent

2 dot adjacent

2 dot adjacent (vertical)

2 dot adjacent (sla
</td></tr>
<tr><td>4.0 Line Defect (LCD /Polarizer backlight black/white line, scratch, stain)</td><td>
<table>
<tr><th rowspan="2">Width (mm)</th><th rowspan="2">Length (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>W ≤ 0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05 < W ≤ 0.06</td><td>L ≤ 5.0</td><td colspan="2">N ≤ 3</td></tr>
<tr><td>0.06 < W ≤ 0.08</td><td>L ≤ 4.0</td><td colspan="2">N ≤ 2</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td rowspan="2"> 
W: width, L：length

N：Count</td><td><table><tr><td>W > 0.08</td><td>Defined as spot defect</td></tr></table></td></tr>
<tr><td>5.0 Electronic Components SMT.</td><td>Not allow missing parts, solderless connection, cold solder joint, mismatch, the positive and negative polarity opposite.</td></tr>
<tr><td>6.0 Display color & Brightness</td><td>1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td></tr>
<tr><td>7.0 LCD Mura/Waving/Hot spot</td><td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td></tr>
<tr><td>8.0 CTP Related</td><td>1. CTP Cover sensor accidented black/white spot<table><tr><th rowspan="2">Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ ≤ 0.15</td><td>Ignore</td><td rowspan="4" colspan="2">Ignore</td></tr><tr><td>0.15 < Φ ≤ 0.25</td><td>4 (distance ≥ 10mm)</td></tr><tr><td>0.25 < Φ ≤ 0.35</td><td>3 (distance ≥ 10mm)</td></tr><tr><td>Φ > 0.35</td><td>0</td></tr></table>2. CTP Cover Strach<table><tr><th rowspan="2">Width (mm)</th><th rowspan="2">Length (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>W ≤ 0.05</td><td>Ignore</td><td colspan="3">Ignore</td></tr><tr><td>0.05 < W ≤ 0.06</td><td>L ≤ 4.0</td><td colspan="3">N ≤ 3</td></tr><tr><td>0.06 < W ≤ 0.08</td><td>L ≤ 3.0</td><td colspan="3">N ≤ 2</td></tr><tr><td>W > 0.08</td><td colspan="4">Defined as spot defect</td></tr></table>3. CTP Cover Pinhole/ Lack of ink<table><tr><th>Size</th><th>C zone acceptable Qty</th></tr><tr><td>Φ ≤ 0.2</td><td>Ignore</td></tr><tr><td>0.2 < Φ ≤ 0.3</td><td>4 (distance ≥ 10mm)</td></tr><tr><td>0.3 < Φ ≤ 0.4</td><td>2 (distance ≥ 10mm)</td></tr><tr><td>Φ > 0.4</td><td>0</td></tr></table>4. CTP Bonding bubble/accidented spot<table><tr><th rowspan="2">Size Φ (mm)</th><th colspan="2">Acceptable Qty</th></tr><tr><th>A</th><th>B</th></tr></table></td></tr>
</table>

Φ ≤ 0.1	Ignore
0.1 < Φ ≤ 0.2	3 (distance ≥ 10mm)
0.2 < Φ ≤ 0.3	2 (distance ≥ 10mm)
Φ > 0.3	0

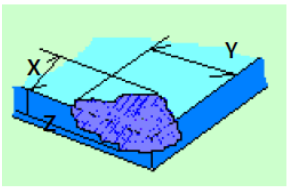
5. Assembly deflection

beyond the edge of backlight ≤ 0.2mm

6. CTP cover broken

X: length, Y: width, Z: height

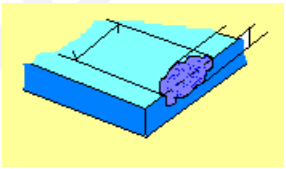
X	Y	Z
X ≤ 0.5mm	Y ≤ 0.5mm	Z < cover thickness



Circuitry broken is not allowed

7. CTP cover broken

X: length, Y: width, Z: height



Circuitry broken is not allowed

Criteria (functional items)

No	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight	Not allowed
5	CTP no function	Not allowed

8.4 Dealing with Customer Complaints

8.4.1 Non-conforming Analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in reasonable time and update the status to the purchaser.

8.4.2 Handling of Non-conforming Displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

9. Reliability Specification

9.1 Reliability Tests

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C, 96 hours	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD. 2.Non-display. 3.Missing segments/line. 4.Glass crack. 5.Current IDD is twice higher than initial value.
Low Temperature Operation	-20°C, 96 hours	
High Temperature Storage	80°C, 96 hours	
Low Temperature Storage	-30°C, 96 hours	
Damp Proof Test	60°C, 90%RH, 96 hours	
Thermal Shock (Non-operation)	-20°C, 30 min ↔ 70°C, 30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330, 5points/panel Air: ±8KV, 5times; Contact: ±6KV, 5 times. (Environment: 15°C ~35°C, 30% ~ 60%).	
Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.5mm Sweep:10Hz ~ 55Hz ~ 10Hz, 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition)	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm (MEDIUM BOX)	

Note 1: The test samples should be applied to only one test item.

Note 2: Sample size for each test item is 5~10pcs.

Note 3: For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.

Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

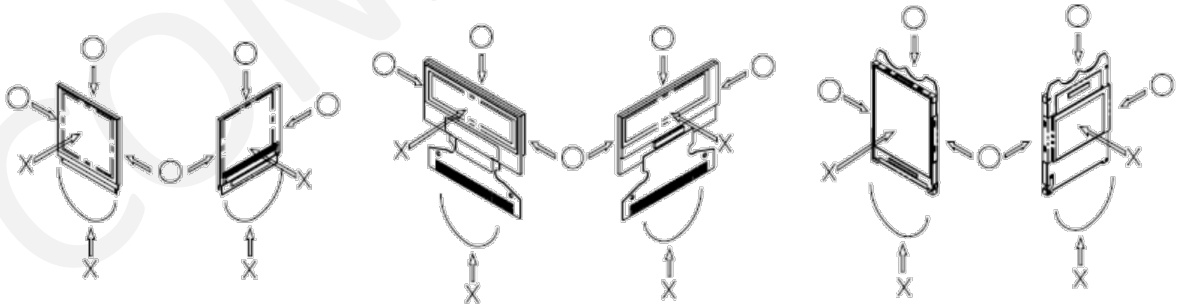
Note 5: Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

Note 6: The color fading mura of polarizing filter should not care.

10. Handling Precautions

10.1 Handling Precautions

1) Since the display panel is made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water
4) If pressure is applied to the display surface or its neighbourhood of the display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
5) The polarizer covering the surface of the display module is soft and easily scratched. Please be careful when handling the display module.
6) When the surface of the polarizer of the display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   a. Scotch Mending Tape No. 810 or an equivalent
   b. Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   c. Also, pay attention that the following liquid and solvent may spoil the polarizer:
      - Water
      - Ketone
      - Aromatic Solvents
7) Hold the display module very carefully when placing it into the system housing. Do not apply excessive stress or pressure to display module. And, do not over bend the film with electrode pattern layouts. These stresses will



influence the display performance. Also, secure sufficient rigidity for the outer cases.
8) Do not apply stress to the LSI chips and the surrounding molded sections.
9) Do not disassemble nor modify the display module.
10) Do not apply input signals while the logic power is off.
11) Pay sufficient attention to the working environments when handing display modules to prevent occurrence of element breakage accidents by static electricity.
    a. Be sure to make human body grounding when handling display modules.

b. Be sure to ground tools to use or assembly such as soldering irons.
c. To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
d. Protective film is being applied to the surface of the display panel of the display module. Be careful since static electricity may be generated when exfoliating the protective film.

12) A Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. If the display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
13) If electric current is applied when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

10.2 Storage Precautions

1) When storing display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you store these modules in the packaged state when they are shipped from Densitron) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the display module, when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

10.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for display module, and if these values are exceeded, panel damage may happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the display module, fasten the external plastic housing section.
7) If power supply to the display module is forcibly shut down by such errors as taking out the main battery while the display panel is in operation, we cannot guarantee the quality of this display module.

10.4 Operation Precautions

1) It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.
2) Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation.
3) Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged.
4) To protect display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the display modules.
   a. Pins and electrodes
   b. Pattern layouts such as the FPC
5) When the driver is being exposed (COG), semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if the driver is exposed to light, malfunctioning may occur.
   a. Design the product and installation method so that the driver may be shielded from light in actual usage.
   b. Design the product and installation method so that the driver may be shielded from light during the inspection processes.
6) Although the display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from the influences of noise on the system design.
7) We recommend you construct its software to make periodical refreshments of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

10.5 Cleaning Precautions

1) Keep TFT Scratch free: Avoid using abrasive materials like paper towels and newspaper in cleaning TFT LCD screens as they may scratch the surface. Instead, opt for a lint-free cloth. Don't spray the liquid directly on the monitor and remember to put gentle pressure when wiping the screen.

2) Avoid Vibration: During cleaning process, try to keep the TFT on shock proof platform to avoid strong shock and vibration. Do not apply pressure to the LCD screen of the LCD or bump or squeeze the LCD display back cover.

3) When the surface of the polarizer of the display module has soil, clean the surface. It takes advantage of using the following adhesion tape:

   a) Scotch Mending Tape No. 810 or an equivalent.

   b) Never try to breathe upon the soiled surface.

   c) List of Safe and Unsafe solvents to clean TFT display:

Safe Solvents	Unsafe Solvents
Distilled Water	Ammonia
Isopropyl Alcohol	Acetone
Diluted White Vinegar = Water (Mix 1 part vinegar + 5 parts of Water)	Ethyl Alcohol
	Methyl Chloride
	Ethyl Acid

10.6 Other Precautions

1) Request the qualified companies to handle industrial wastes when disposing of the display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.