DMT080H4NMNT0-2A
PRODUCT SPECIFICATION

Version 0.1
Nov 29, 2022

TBD

Customer's Approval	
Signature	*Date*

Prepared by Victoria *Ho*
Approved by *Eric Wan*

Revision History

VERSION	DATE	DESCRIPTION	AUTHOR
0.1	Nov 29, 2022	Preliminary	Victoria Ho

Legal Notice

Table of Contents

1. General Description

1.1 Introduction

This is a 8” size colour active matrix TFT LCD module that uses amorphous silicon TFT as a switching device. The display is normally black mode, transmissive, and featuring high contrast and excellent colour saturation. The resolution of the TFT-LCD is 800 x 1280 and can display up to 16.7M colours. The display module supports MIPI interface.

1.2 Main Features

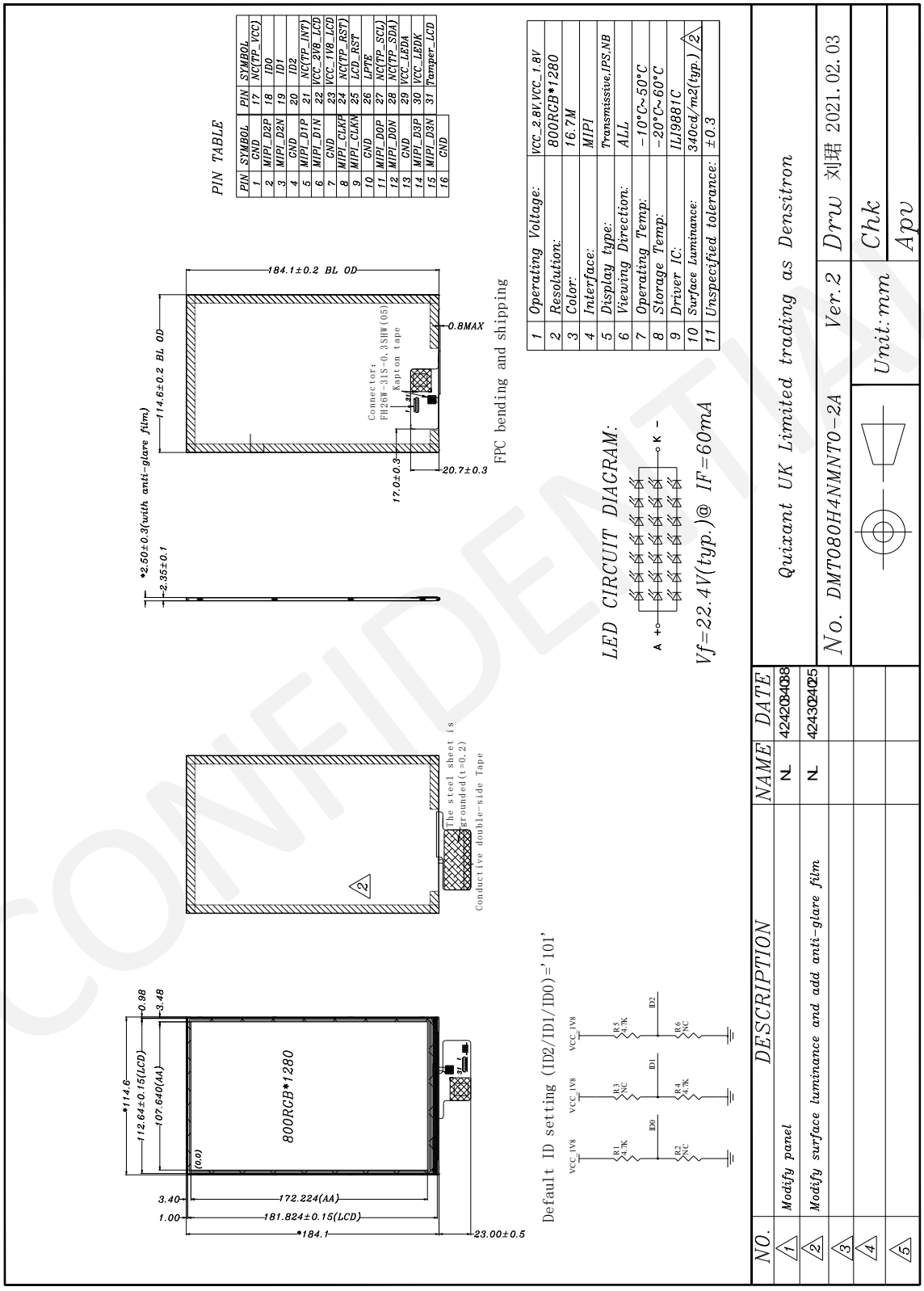
Item	Contents
Display Type	TFT LCD
Screen Size	8.0” Diagonal
Display Format	800 x RGB x 1280 Dots
No. of Colour	16.7M
Overall Dimensions	114.6 (W) x 184.1 (H) x 2.5 (D) mm
Active Area	107.64 (W) x 172.224 (H) mm
Mode	Normally Black / Transmissive / IPS
Surface Treatment	Anti-Glare (3H)
Viewing Direction	All round
Interface	MIPI
Driver IC	ILI9881C
Backlight Type	LED, White, 21 chips
Operating Temperature	-10°C ~ +50°C
Storage Temperature	-20°C ~ +60°C
ROHS	Compliant to RoHS 2.0

2. Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Display Format	800 x RGB x 1280	Dots
Overall Dimensions	114.6 (W) x 184.1 (H) x 2.5 (D)	mm
Active Area	107.64 (W) x 172.224 (H)	mm
Dot Pitch	0.13455 (W) x 0.13455 (H)	mm
Weight	TBD	g
IC Controller/Driver	ILI9881C	

2.2 Mechanical Drawing



3. Electrical Specification

3.1 Absolute Maximum Ratings

AGND = GND = 0V, Ta = 25℃

Item	Symbol	Min	Max	Unit	Note
Power Voltage	VCC_2.8V	2.5	6.0	V	-
	VCC_1.8V	1.75	3.3	V	-
Operating Temperature	T_{OP}	-10	50	°C	-
Storage Temperature	T_{ST}	-20	60	°C	-

Note 1: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. For normal operations, it is desirable to use this module under the conditions according to Section 3.2 “Electrical Characteristics”, to avoid malfunctioning.

Note 2: Background colour changes slightly depending on ambient temperature. This phenomenon is reversible.

Note 3: Please refer to item of RELIABILITY.

3.2 Electrical Characteristics

3.2.1 Recommended Operating Condition

(AGND = GND = 0V, Ta = 25℃)

Item	Symbol	Min	Typ.	Max	Unit	Note
Power Voltage	VCC_2.8V	2.5	2.8	6.0	V	-
	VCC_1.8V	1.75	1.8	3.3	V	-
	VDDI	1.65	2.8	3.3	V	
Input Logic High Voltage	VIH	0.7 IOVCC	-	IOVCC	V	-
Input Logic Low Voltage	VIL	-0.3	-	0.3 IOVCC	V	-

3.3 Interface Pin Assignment

3.3.1 TFT PIN Define

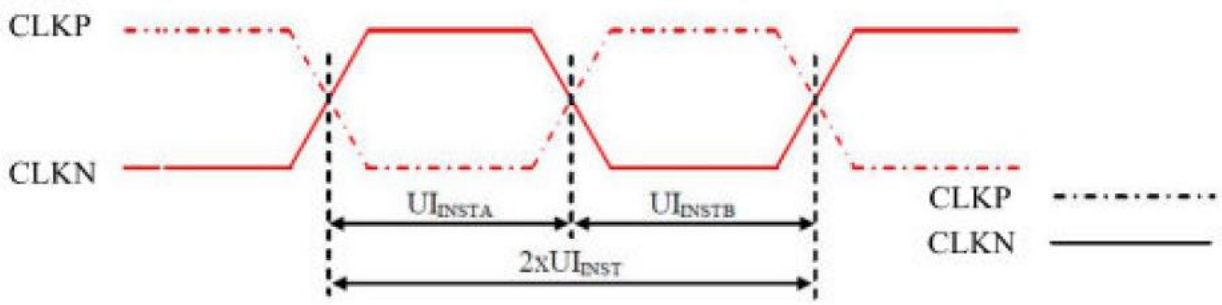
No.	Symbol	I/O	Function
1	GND	P	Ground
2	MIPI_D2P	I	MIPI DSI differential data pair. (Data lane 2)
3	MIPI_D2N	I	
4	GND	P	Ground
5	MIPI_D1P	I	MIPI DSI differential data pair. (Data lane 1)
6	MIPI_D1N	I	
7	GND	P	Ground
8	MIPI_CLKP	I	MIPI DSI differential clock pair
9	MIPI_CLKN	I	
10	GND	P	Ground
11	MIPI_D0P	I	MIPI DSI differential data pair. (Data lane 0)
12	MIPI_D0N	I	
13	GND	P	Ground
14	MIPI_D3P	I	MIPI DSI differential data pair. (Data lane 3)
15	MIPI_D3N	I	
16	GND	P	Ground
17	TP_VCC	P	TP power voltage
18	ID0	-	ID0
19	ID1	-	ID1
20	ID2	-	ID2
21	TP_INT	P	TP external interrupt to the host

No.	Symbol	I/O	Function
22	VCC_2V8_LCD	P	Power supply
23	VCC_1V8_LCD	P	Power supply
24	TP_RST	P	TP reset input pin
25	LCD_RST	P	LCD reset
26	LPTE	O	Tearing Effect pin.
27	TP_SCL	P	TP clock signal
28	TP_SDA	P	TP data signal
29	VCC_LEDA	P	LED anode
30	VCC_LEDK	P	LED cathode
31	Tamper_LCD	-	Tamper_LCD

3.4 Timing Characteristics

3.4.1 AC Electrical Characteristics

High Speed Mode – Clock Channel Timing



DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

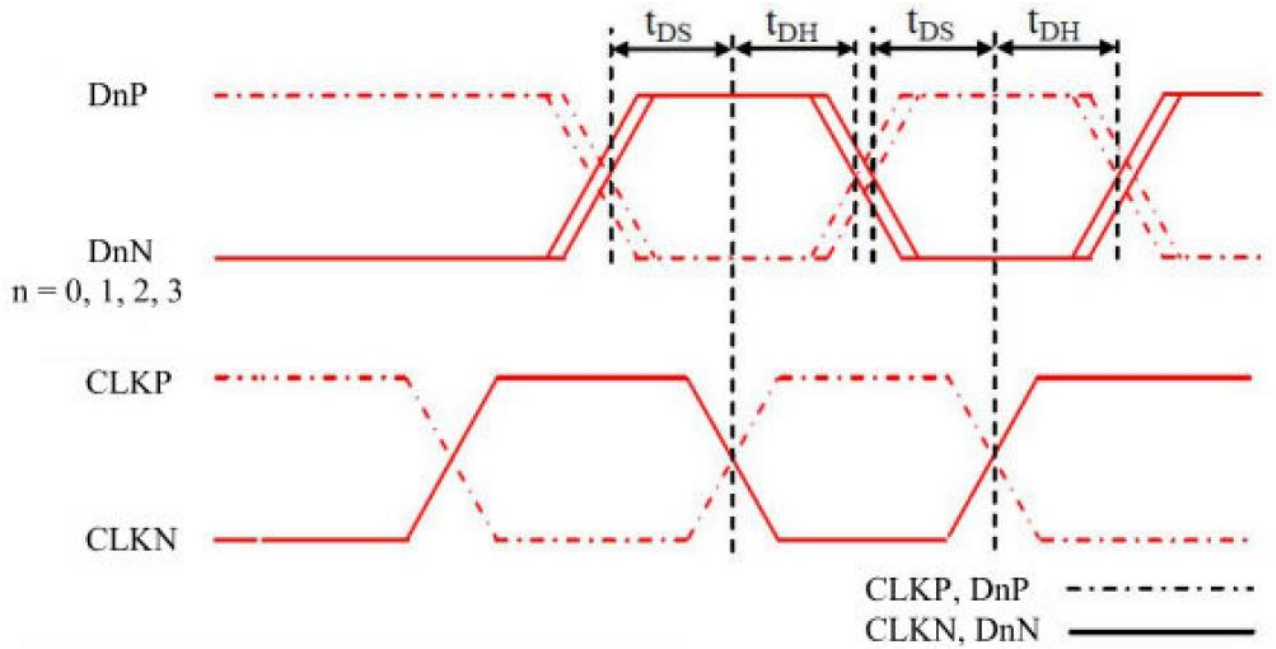
Note 1: $UI=UI_{INSTA}=UI_{INSTB}$

Note 2: Define the minimum value of 24 UI per Pixel.

Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

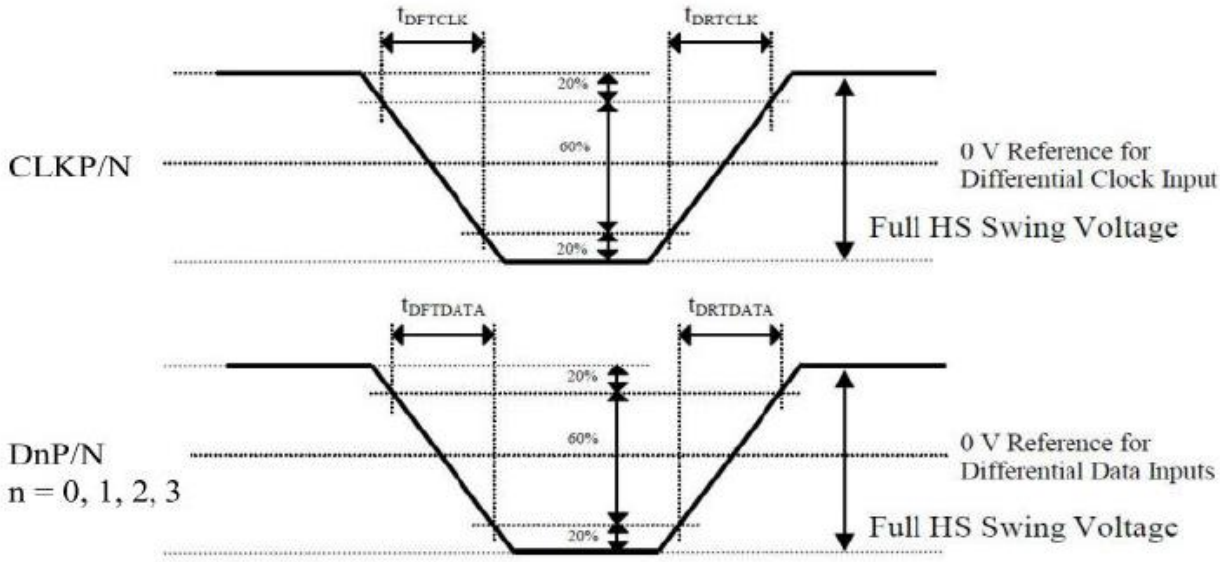
High Speed Mode – Data Clock Channel Timing



DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max	Unit
DnP/N, n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-	-

High Speed Mode – Rising and Falling Timings



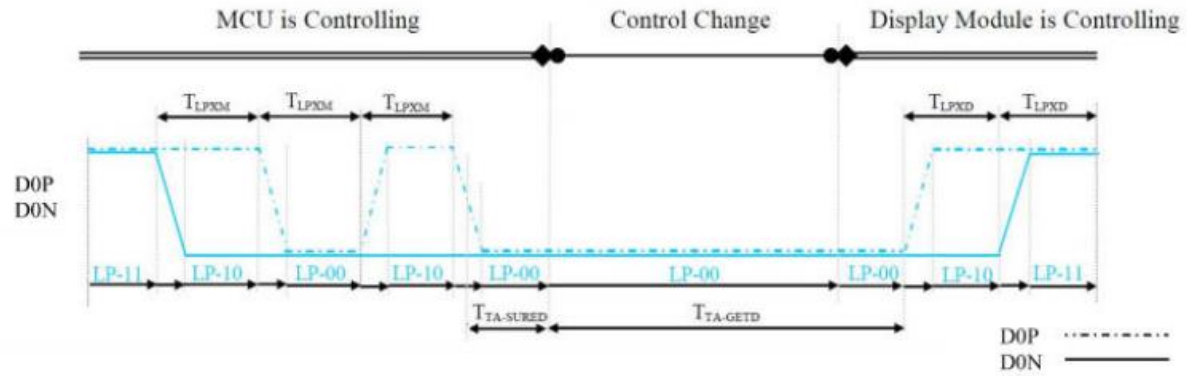
Parameter	Symbol	Condition	Min	Typ.	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3 UI
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3 UI
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3 UI
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3 UI

Note: The display module has to meet timing requirements, what are defined for the transmitter (MCU) on MIPI D-Phy standard.

Low Speed Mode – Bus Turn Around

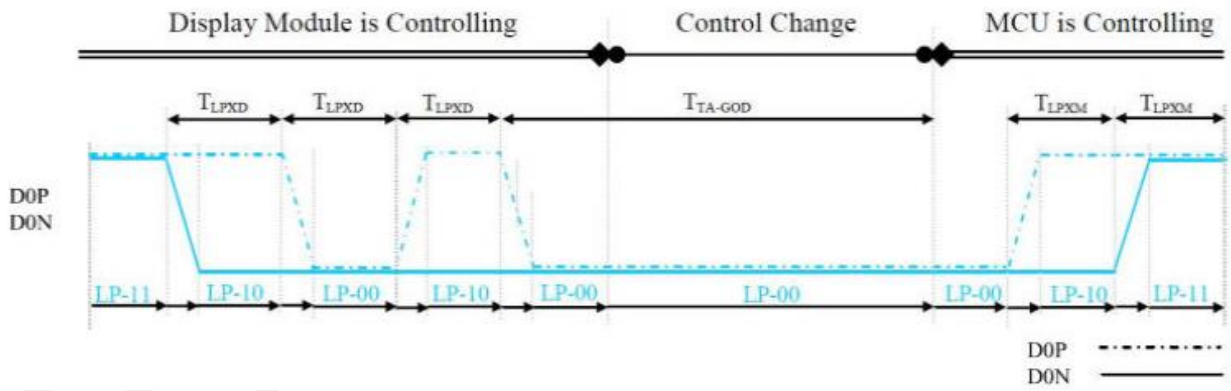
Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

BTA from the MCU to the Display Module



Lower Power Mode and its State Periods on the Bus Turnaround (BTA)from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

BTA from the Display Module to the MCU



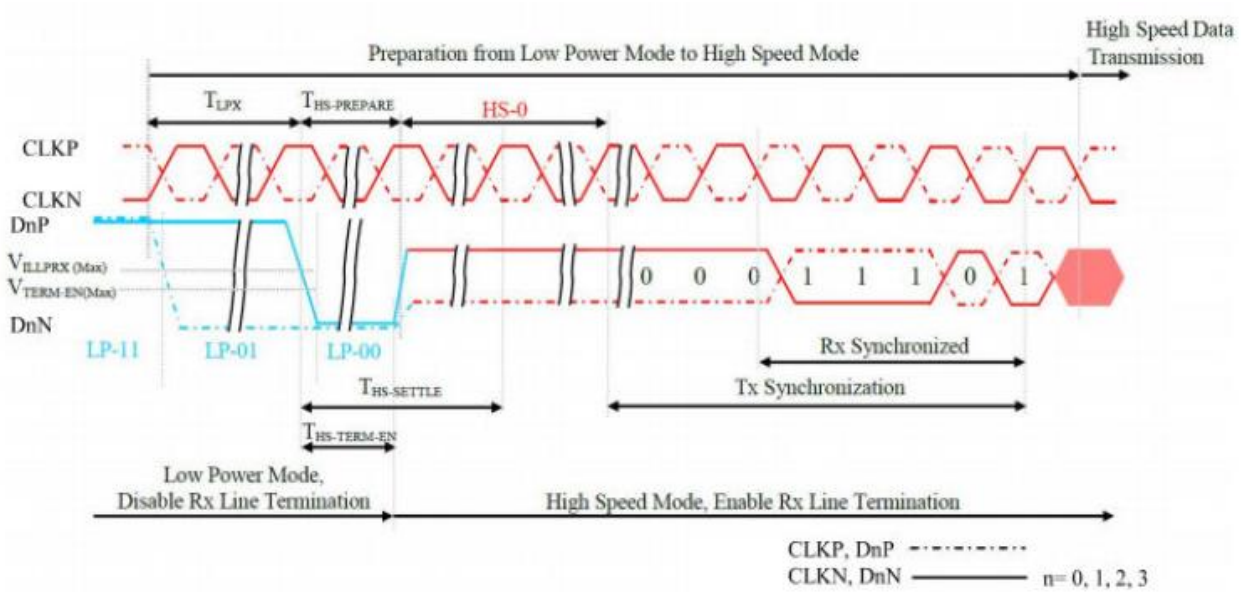
Low Power State Period Timings - A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (LI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (LI9881C) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (LI9881C) starts driving	T_{LPXD}	2 x T_{LPXD}	ns

Low Power State Period Timings – B

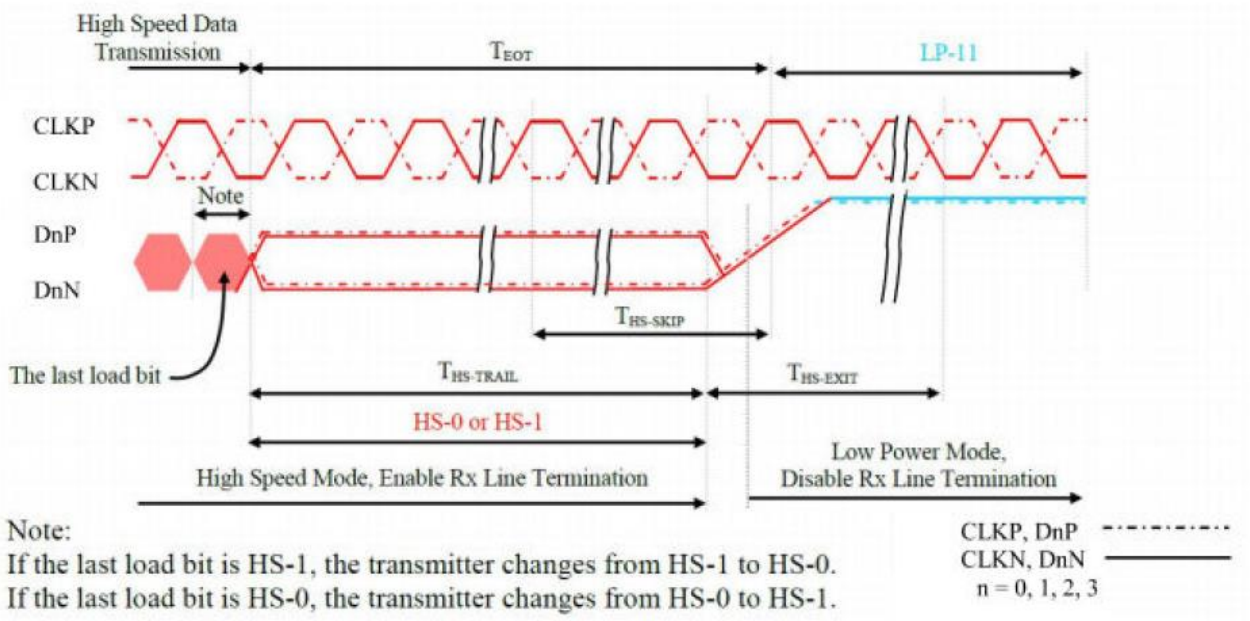
Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (LI9881C)	5 x T_{LPXD}	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MCU	4 x T_{LPXD}	ns

Data Lanes from Low Power Mode to High Speed Mode



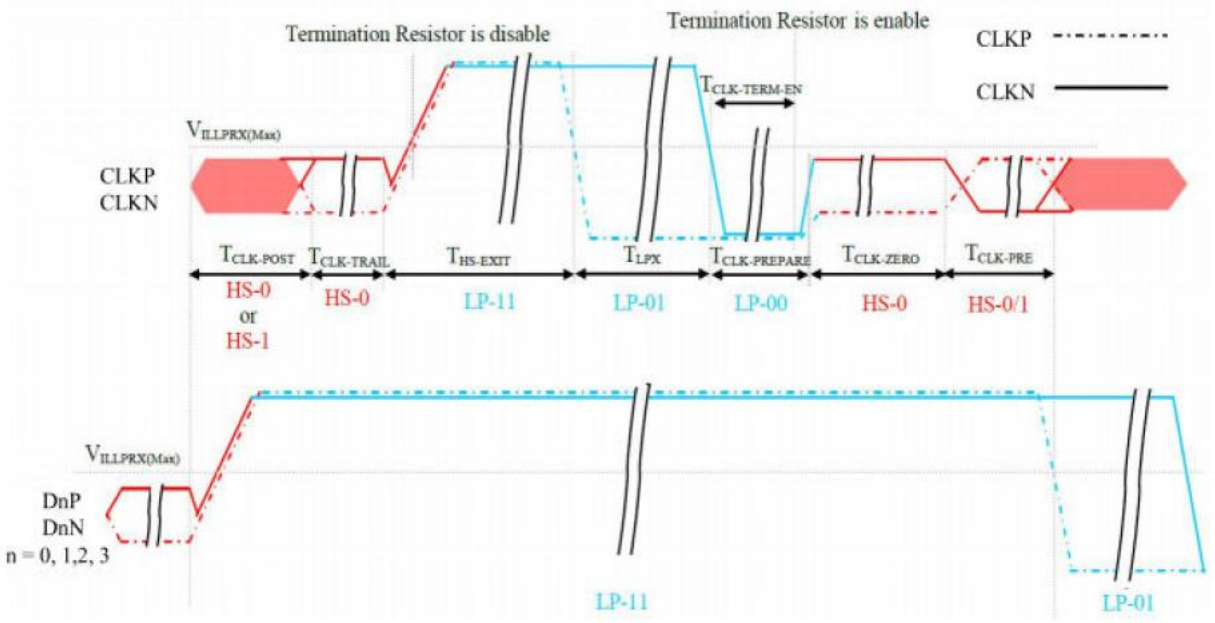
Signal	Symbol	Description	Min	Max	Unit
DnP/N, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Data Lanes from High Speed Mode to Low Power Mode



Signal	Symbol	Description	Min	Max	Unit
DnP/N, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (LI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

Clock Lanes-High Speed Mode to/from Low Power Mode Timings



Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the test associated to LP mode.	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-10 to prepare for HS termination	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

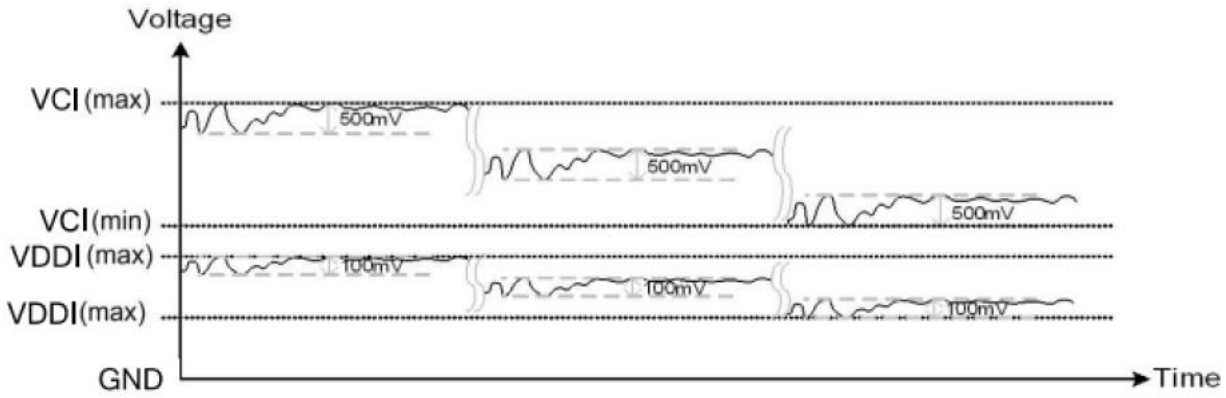
3.4.2 DC Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Analog Power Supply Voltage	VCI	Operating Voltage	2.5	2.8	6.0	V
Digital Power Supply Voltage	VDDI	Operating Voltage	1.65	1.8	3.3	V
Analog Power Supply Voltage Noise	V_{VCI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV
		Noise Range, 0 to 30KHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV
Digital Power Supply Voltage Noise	V_{VDDI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Note 1: Ta=-30℃ to 70℃ (to +85℃ no damage)

Note 2: These values are not symmetric amplitude, which center points are VDDI or VCl. See examples, when VVCI_NOISE and VVDDI_NOISE are maximums, as reference purposes below.

Noise on Power Supply Lines



DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10and LP-11 are defined in the table below:

DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV	3
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV	3
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1, D2, D3)	880	-	1350	mV	3
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1, D2, D3)	0.0	-	550	mV	3
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP Mode)	0.0	-	300	mV	3
Logic 1 output current	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V	3
Logic 0 output current	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV	3
Logic 1 Input Current	I_{IH}	LP-CD, LP-RX	-	-	10	uA	3
Logic 0 Input Current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA	3

Note 1: Ta=-30℃ to 70℃ (to +85℃ no damage)

Note 2: DSI High Speed mode is off

DC Characteristics for DSI HS Mode

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N	70	-	330	mV	2,3
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N	70	-	330	mV	2, 3, 5
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N	-50	-	50	mV	4
Common Mode Ripple for Data Equal or Less than 450 MHz	$V_{CMRDATAL450}$	DnP/N	-50	-	50	mV	4, 5
Common Mode Ripple for Clock More than 450 MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV	-
Common Mode Ripple for Data More than 450 MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N	-	-	100	mV	5
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV	-
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA+}$	DnP/N	-70	-	-	mV	5
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV	-
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N	-	-	70	mV	5
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, DnP/N	-40	-	-	mV	3, 5
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, DnP/N	-	-	460	mV	3, 5
Differential Termination Resistor	R_{TERM}	CLKP/N, DnP/N	80	100	125	Ω	5
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N	-	-	450	mV	5
Termination Capacitor	C_{TERM}	CLKP/N, DnP/N	-	-	60	pF	5, 6

Note 1: Ta = -30℃ to 70℃ (to +85℃ no damage), VCI = 2.5V to 6.0V, VDDI = 1.65 to 3.3V

Note 2: Includes 50mV (-50mV to 50mV) ground difference.

Note 3: Without VCMRCLKM450/VCMRDATAM450.

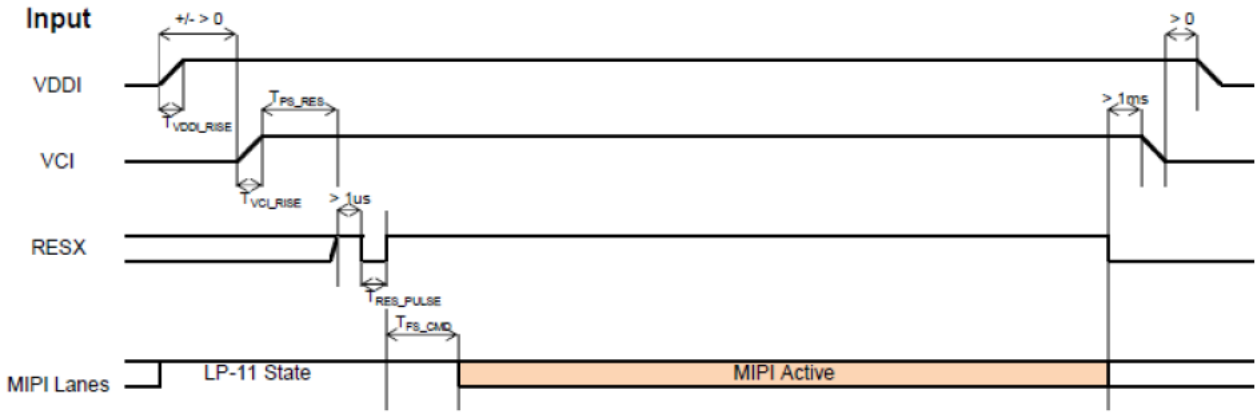
Note 4: Without 50mV (-50mV to 50mV) ground difference.

Note 5: n = 0 and 1.

Note 6: For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

3.4.3 Power On/Off Sequence

Power Mode 3



Item	Symbol	Min	Typ.	Max	Unit
VDDI Rise time	T_{VDDI_RISE}	200	-	-	µs
VCI Rise time	T_{VCI_RISE}	200	-	-	µs
VDDI/VCI on to Reset high	T_{PS_RES}	5	-	-	Ms
Reset low pulse time	T_{RES_PULSE}	10	-	-	µs
Reset to first command	T_{FS_CMD}	10	-	-	ms

4. Optical Specification

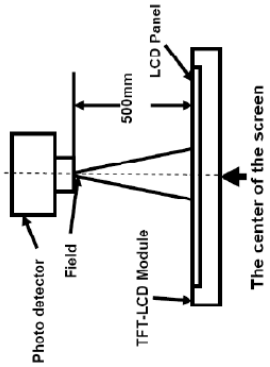
4.1 Optical Characteristics

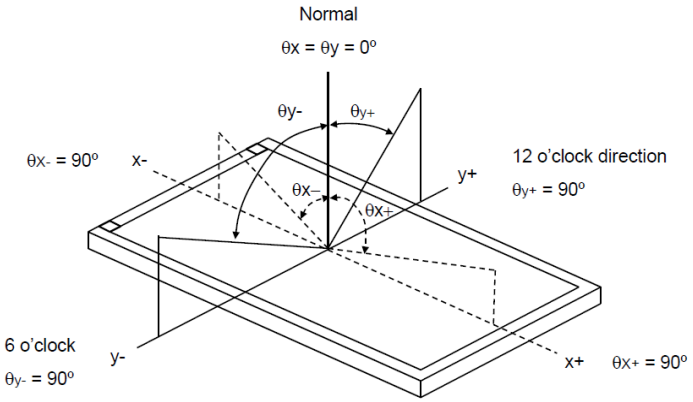
Characteristics		Symbol	Conditions	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	θ = 0° Normal viewing angle	900	1200	-	-	1, 3
Response time		TR + TF		-	-	35	ms	1, 4
Viewing Angle	Left	θ_x-	CR>10	-	80	-	deg	2
	Right	θ_x+		-	80	-		
	Up	θ_Y+		-	80	-		
	Down	θ_Y-		-	80	-		
Colour Chromaticity	Red	Rx	θ = 0° Normal viewing angle	0.591	0.621	0.651	-	1, 5
		Ry		0.332	0.362	0.392		
	Green	Gx		0.285	0.315	0.345		
		Gy		0.575	0.605	0.635		
	Blue	Bx		0.124	0.154	0.184		
		By		0.060	0.090	0.120		
	White	Wx		0.259	0.289	0.319		
		Wy		0.283	0.313	0.343		
Luminance		Lv	I_F = 60mA	-	340	-	cd/m^2	5

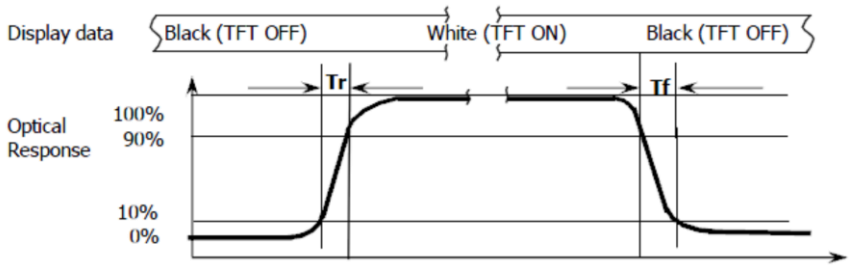
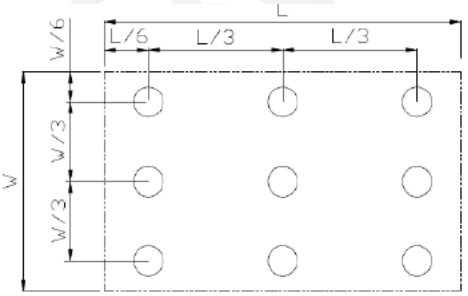
Conditions:

1. If=60mA(Backlight current), VCC_2.8V = 2.8V, the ambient temperature is 25°C.

2. The test systems refer to Note 2.

<table>
<tr><th>Note</th><th>Item</th><th>Test method</th></tr>
<tr><td>1</td><td>Definition of optical measurement system</td><td>The optical characteristics should be measured in dark room. After 5Minutes operation, the optical properties are measured at the center point of the LCD screen. ALL input terminals LCD panel must be ground when measuring the center area of the panel.
 

<table>
<tr><th>Item</th><th>Photo detector</th><th>Field</th></tr>
<tr><td>Contrast Ratio</td><td rowspan="3">CS1000</td><td rowspan="3">1°</td></tr>
<tr><td>Luminance</td></tr>
<tr><td>Lum Uniformity</td></tr>
<tr><td>Chromaticity</td><td>CS1000</td><td></td></tr>
<tr><td>Response Time</td><td>DMS703</td><td>-</td></tr>
</table></td></tr>
<tr><td>2</td><td>Definition of Viewing Angle (θx, θy)</td><td>Viewing angle is measured at the center point of the LCD by CONOSCOPE (DMS703)
 
</td></tr>
<tr><td>3</td><td>Definition of Contrast Ratio (CR)</td><td>White state: The state is that the LCD should drive by Vwhite.
$$\text{Contrast ratio(CR)}= \frac{\text{Luminance measured when LCD is on the “White” state}}{\text{Luminance measured when LCD is on the “Black” state}}$$
Black state: The state is that the LCD should drive by Vblack.
Vwhite: To be determined Vblack: To be determined</td></tr>
<tr><td>4</td><td>Definition of Response Time (T_R, T_F)</td><td>The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF})is the time between photo detector output intensity changed from 10% to90%.</td></tr>
</table>

Note	Item	Test method
		
5	Definition of color chromaticity （CIE1931）	Color coordinates measured at center point of LCD.
6	Definition of Luminance Uniformity	Active area is divided into 9 measuring areas(Refer Fig.2).Every measuring point is placed at the center of each measuring area. Luminance Uniformity (U)=Lmin/Lmax L-Active area length W-Active area width  L max: The measured Maximum luminance of all measurement position. L min: The measured Minimum luminance of all measurement position.
7	Definition of luminance	Measure the luminance of white state at center point.

5. LED Backlight Specification

5.1 LED Backlight Characteristics

Ta = 25℃

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Forward Voltage	Vf	-	-	22.4	-	V	-
Forward Current	If	-	-	60	-	mA	-
Operating Lifetime	-	-	30000	-	-	Hours	1, 2

Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: If the module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.

Note 3: Operating life means brightness goes down to 50% initial brightness. Minimum operating life time is estimated data.

5.2 INTERNAL CIRCUIT DIAGRAM

Vf=22.4V (typ.) @ If=60mA

6. Packaging

CUSTO MER'S APPROVED:	DATE: 2020.12.17	PAGE: 1/1

PRODUCT PART NO.: DMT080H4NMNT0-2A

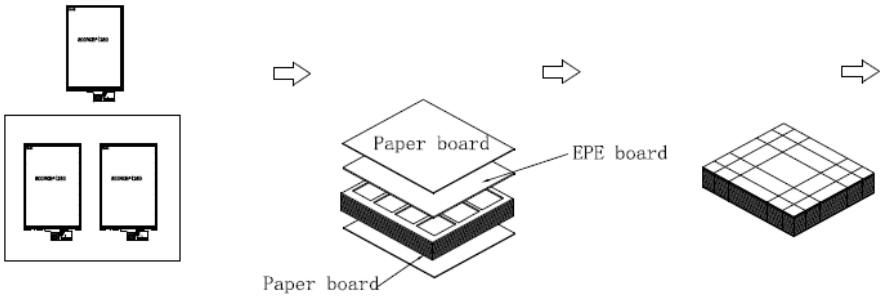
PACKING TYPE: BY EPE TRAY

PACKLING ORDER:

1) Putting 2 pcs Modules on each EPE tray.

2) Putting 8 pcs EPE trays together with EPE paper on the top of EPE tray.

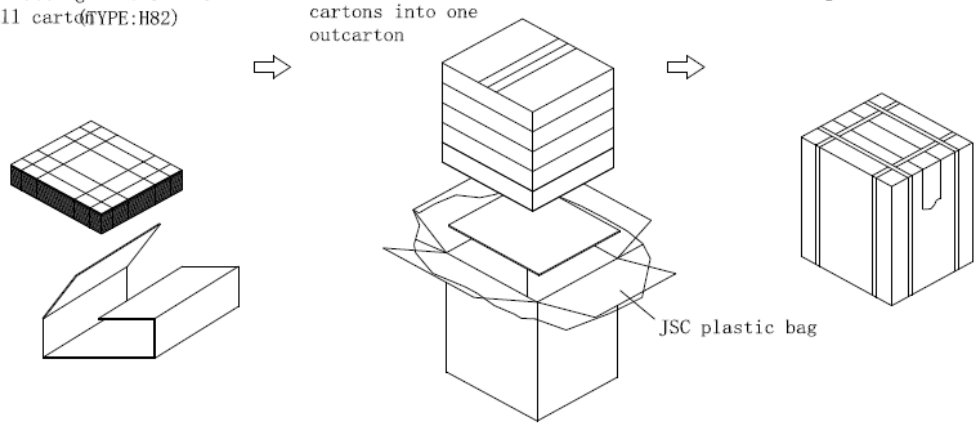
3) Assembling the boards and the tray together with adhesive tape



4) Putting in the inner small carton(TYPE:H82)

5) Putting 5 small cartons into one outcarton

6) Packing finished



Note: 2 pcs in a tray, 8 trays in a inner carton, 5 inner cartons in a out carton, 2x8x5=80pcs/Outcarton

Dimension (Small carton) 385*325*87mm

Dimension (Out carton) 394*344*470mm

NO. DMT080H4NMNT0-2A	Drw:		Chk:		Apv:	

Quixant UK Limited trading as Densitron

7. Quality Assurance Specification

7.1 Conformity

The performance, function and reliability of the shipped products conform to the Product Specification.

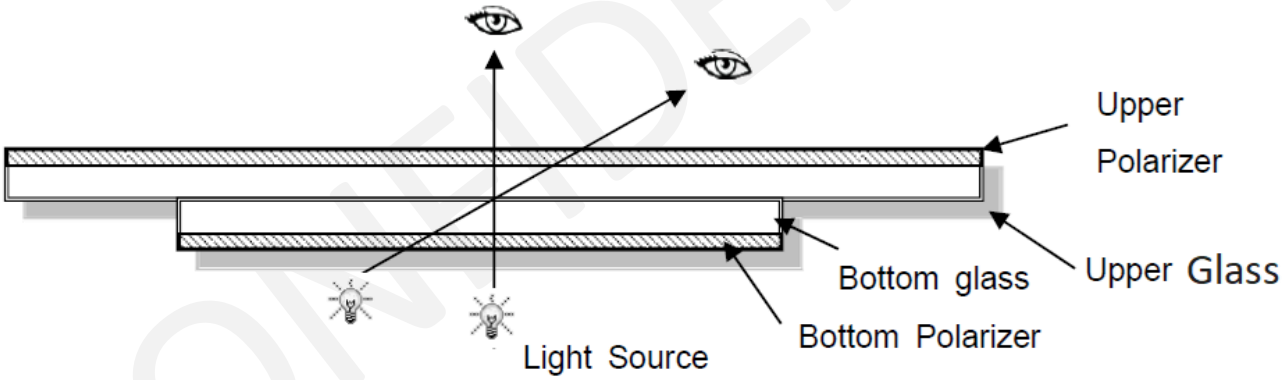
7.2 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	25 ± 5°C
Humidity:	65% ± 5% RH
Viewing Angle:	Normal Viewing Angle
Illumination:	under 40W fluorescent light
Viewing distance:	35± 5cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

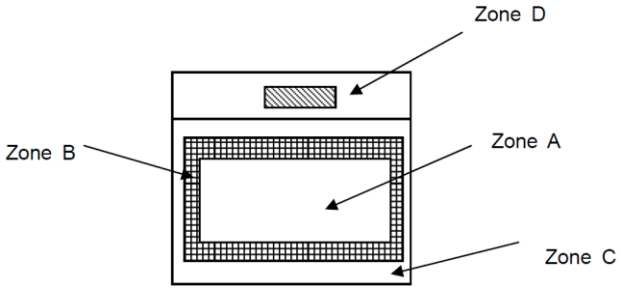


7.3 Delivery Assurance

7.3.1 Delivery Inspection Standards

Class II, Normal Inspection, MIL-STD-105E

7.3.2 Zone Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A + Zone B) Area which cannot be seen after assembly by customer.

Zone D: IC Bonding Area

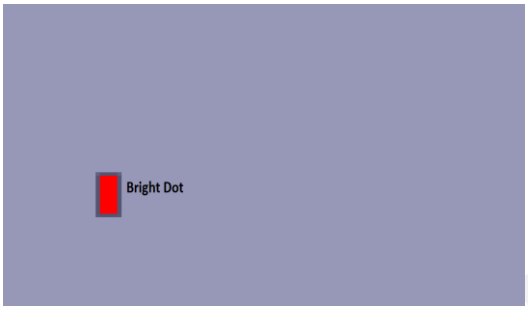
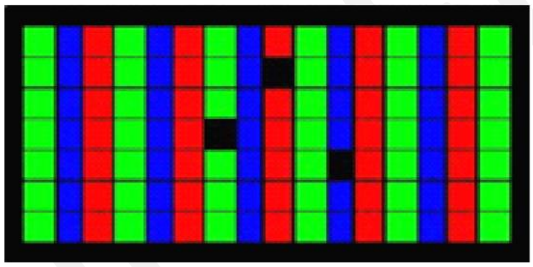
Note: Generally, visual defects in Zone C can be ignored when it doesn't affect product function or appearance after assembly by customer

7.3.3 Criteria & Acceptable Quality Level

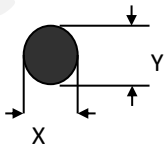
Partition	AQL	Definition
Major (MA)	0.65	1. Liquid crystal leakage 2. Wrong polarizer 3. Outside dimension 4. Bright dot, dark dot 5. Display abnormal 6. Class crack
Minor (MI)	1.0	1. Spot Defect (Including black spot, white spot, pinhole, foreign particle, bubbles, hurt) 2. Fragment 3. Line Defect (Including black line, white line, scratch) 4. Incision defect 5. Newton's ring 6. Other visual defects

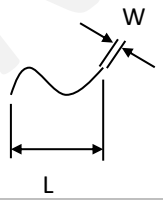
7.3.4 Criteria & Classification

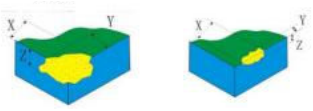
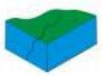
7.3.4.1 Bright/ Dark Dots Explain

Name	Explain	Definition
Bright dot	Dots bright and unchanged in size in which LCD panel is displaying black pattern 	The definition of dot: The size of a defective dot over 1/2 of single pixel dot is regarded as one defective dot. Note: One pixel consists of 3 sub-pixels, including R, G, and B dot. (Sub-pixel=Dot)
Dark Dot	Dots appear dark and unchanged in size in which LCD panel is displaying pure red, green, blue pattern 	
Accidented Dot	Adjacent two sub-pixel are defect (define two dot defect)	

7.3.4.2 Inspection Standard

Class	Item	Criteria
Major	Bright / Dark Dot	1) LCD≤4.3"
		Bright dot: N≤2, Dark dot: N≤3, Total: N≤4
		2) 4.3"＜LCD＜7"
		Bright dot: N≤3, Dark dot: N≤4, Total: N≤6
		3) 7"≤LCD≤12"
		Bright dot: N≤4, Dark dot: N≤5, Total: N≤8
		4) LCD＞12"
		Bright dot: N≤5, Dark dot: N≤6, Total: N≤10
		The distance between the two defect dots shall be greater than 5mm The distance between two defect dots above 7 inches shall be more than 10 mm **Note:** Adjacent dot defect N≤0
Minor	Spot Defects (Black spot, white spot, Pinhole, foreign matter, dent, backlight foreign matter）	Round type: as per following drawing, ∅ = (X+Y)/2 
		1) LCD≤4.3"
		D≤0.15, Ignore 0.15＜D≤0.3, N≤3 0.3＜D, N=0
		2) 4.3"＜LCD＜7"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤4 0.5＜D, N=0
		3) 7"≤LCD≤12"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤5 0.5＜D, N=0
		4) LCD＞12"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤6 0.5＜D, N=0
Minor	Bubble	1) LCD≤4.3"
		D≤0.2, Ignore

Class	Item	Criteria
		0.2＜D≤0.5, N≤3 0.5＜D, N=0
		2) 4.3"＜LCD＜7"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤4 0.5＜D, N=0
		3) 7"≤LCD≤12"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤5 0.5＜D, N=0
		4) LCD＞12"
		D≤0.2, Ignore 0.2＜D≤0.5, N≤6 0.5＜D, N=0
Minor	Line Defect (Black/white line, backlight foreign matter)	Line type: as per following drawing 
		1) LCD≤4.3"
		W≤0.03, Ignore 0.03＜W≤0.06, L≤5, N≤3 W＞0.06, L＞5, N=0
		2) 4.3"＜LCD＜7"
		W≤0.03, Ignore 0.03＜W≤0.1, L≤5, N≤4 W＞0.1, L＞5, N=0
		3) 7"≤LCD≤12"
		W≤0.03, Ignore 0.03＜W≤0.1, L≤5, N≤5 W＞0.1, L＞5, N=0
		4) LCD＞12"
		W≤0.03, Ignore 0.03＜W≤0.1, L≤5, N≤6 W＞0.1, L＞5, N=0

Class	Item	Criteria	
Minor	Scratch	1) LCD≤4.3"	
		W≤0.03, Ignore 0.03＜W≤0.2, 1.0＜L≤ 5.0, N≤3 W＞0.2, L＞5 N=0	
		2) 4.3"＜LCD＜7"	
		W≤0.03, Ignore 0.03＜W≤0.2, 1.0＜L≤ 5.0, N≤4 W＞0.2, L＞5, N=0	
		3) 7"≤LCD≤12"	
		W≤0.03, Ignore 0.03＜W≤0.2, 1.0＜L≤ 5.0, N≤5 W＞0.2, L＞5, N=0	
		4) LCD＞12"	
		W≤0.03, Ignore 0.03＜W≤0.2, 1.0＜L≤ 5.0, N≤6 W＞0.2, L＞5, N=0	
Major	Display Abnormal	Not allowed	
Major	Outside Dimension	Accord with drawing	
Major	Glass Crack	Not allowed	
Major	Leak	Not allowed	
Minor	Corner and Side Fragment		1. Comer fragment: X, Y≤1mm Z≤T/2: allowed 2. Side fragment: X≤2.0mm Y≤1mm Z≤T/2: allowed
Major	Crack		NG

7.4 Dealing with Customer Complaints

7.4.1 Non-conforming Analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.

After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.4.2 Handling of Non-conforming Displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8. Reliability Specification

8.1 Reliability Tests

Item	Test Condition	
High Temperature Storage	60±2℃/240 hours	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Sealleak; 3.Non-display; 4.Missing segments; 5.Glass crack; 6.Current Idd is twice higher than initial value.
Low Temperature Storage	-20±2℃/240 hours	
High Temperature Operating	50±2℃/240 hours	
Low Temperature Operating	-10±2℃/240 hours	
Temperature Cycle	-20℃~ 25℃~60℃ × 10cycles (30min.) (5min.) (30min.)	
Damp Proof Test	40℃±5℃×90%RH/240 hours	
Vibration Test	Frequency：10Hz~55Hz~10Hz Amplitude: 1.5mm, X, Y, Z direction for total 3hours (Packing condition)	
Drooping Test	Drop to the ground from 1m height, one time, every side of carton. (Packing condition)	
ESD Test	Voltage: ±8KV R: 330Ω C: 150pF Air discharge, 10time	
	Voltage: ±6KV R: 330Ω C: 150pF Contact discharge, 10time	

Note 1: The test samples should be applied to only one test item.
Note 2: Sample size for each test item is 5~10pcs.
Note 3: For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.
Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
Note 5: Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
Note 6: Please use automatic switch menu (or roll menu) testing mode when test operating mode.

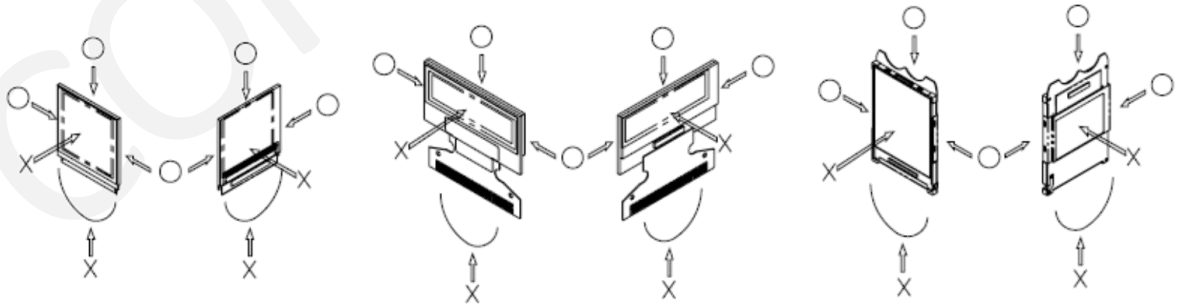
8.1.1 Inspection Check Standard

After the completion of the described reliability test, the samples are to be left at room temperature for 4 hrs prior to conducting the inspection check at 25±5 °C, 65±5% RH.

9. Handling Precautions

9.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water
4) If pressure is applied to the display surface or its neighbourhood of the display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
5) The polarizer covering the surface of the display module is soft and easily scratched. Please be careful when handling the display module.
6) When the surface of the polarizer of the display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   a. Scotch Mending Tape No. 810 or an equivalent
   b. Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   c. Also, pay attention that the following liquid and solvent may spoil the polarizer:
      - Water
      - Ketone
      - Aromatic Solvents
7) Hold the display module very carefully when placing it into the system housing. Do not apply excessive stress or pressure to display module. And, do not over bend the film with electrode pattern layouts. These stresses will



influence the display performance. Also, secure sufficient rigidity for the outer cases.
8) Do not apply stress to the LSI chips and the surrounding molded sections.
9) Do not disassemble nor modify the display module.
10) Do not apply input signals while the logic power is off.
11) Pay sufficient attention to the working environments when handing display modules to prevent occurrence of element breakage accidents by static electricity.

a. Be sure to make human body grounding when handling display modules.
b. Be sure to ground tools to use or assembly such as soldering irons.
c. To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
d. Protective film is being applied to the surface of the display panel of the display module. Be careful since static electricity may be generated when exfoliating the protective film.

12) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. If the display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
13) If electric current is applied when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 Storage Precautions

1) When storing display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the display module, when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the display module, fasten the external plastic housing section.
7) If power supply to the display module is forcibly shut down by such errors as taking out the main battery while the display panel is in operation, we cannot guarantee the quality of this display module.

9.4 Operation Precautions

1) It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.
2) Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation.
3) Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged.
4) To protect display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the display modules.
   a. Pins and electrodes
   b. Pattern layouts such as the FPC
5) When the driver is being exposed (COG), semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if the driver is exposed to light, malfunctioning may occur.
   a. Design the product and installation method so that the driver may be shielded from light in actual usage.
   b. Design the product and installation method so that the driver may be shielded from light during the inspection processes.
6) Although the display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
7) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

9.5 Other Precautions

1) Request the qualified companies to handle industrial wastes when disposing of the display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.