DMT043WVNMCMI-1B
PRODUCT SPECIFICATION

Version 0.1
Sep 19, 2021

TBD

Customer's Approval	
Signature	*Date*

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Revision History

VERSION	DATE	DESCRIPTION	AUTHOR
0.1	Sep 19, 2021	Preliminary	Claudia Wang

Legal Notice

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1. General Description

1.1 Introduction

This is a 4.3” size colour active matrix TFT- LCD that uses amorphous silicon TFT as a switching device. The display is normally black mode, transmissive, and featuring high contrast and excellent colour saturation. The resolution of the TFT-LCD is 480 x 800 pixels and can display up to 65K/262K/16.7M colours. The display module supports MIPI interface and 5 points tape bonding touch panel.

1.2 Main Features

Item	Contents
Display Type	TFT LCD
Screen Size	4.3” Diagonal
Display Format	800 x RGB x 480 Dots
No. of Colour	65K/262K/16.7M
Overall Dimensions	62.50 (H) x 105.55 (V) x 4.20 (D) mm
Active Area	56.16 (H) x 93.60 (V) mm
Mode	Normally Black / Transmissive
Surface Treatment	Anti-Glare (3H)
Viewing Direction	All round
Interface	16/18/24 Bit RGB
Driver IC	ILI9806E
Backlight Type	LED, White, 10 chips
Touch Panel	PCT
Touch Interface	I^2C
Touch Driver IC	GT911
Bonding Type	Tape Bonding
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
ROHS	Compliant to RoHS 2.0

1.3 CTP Features

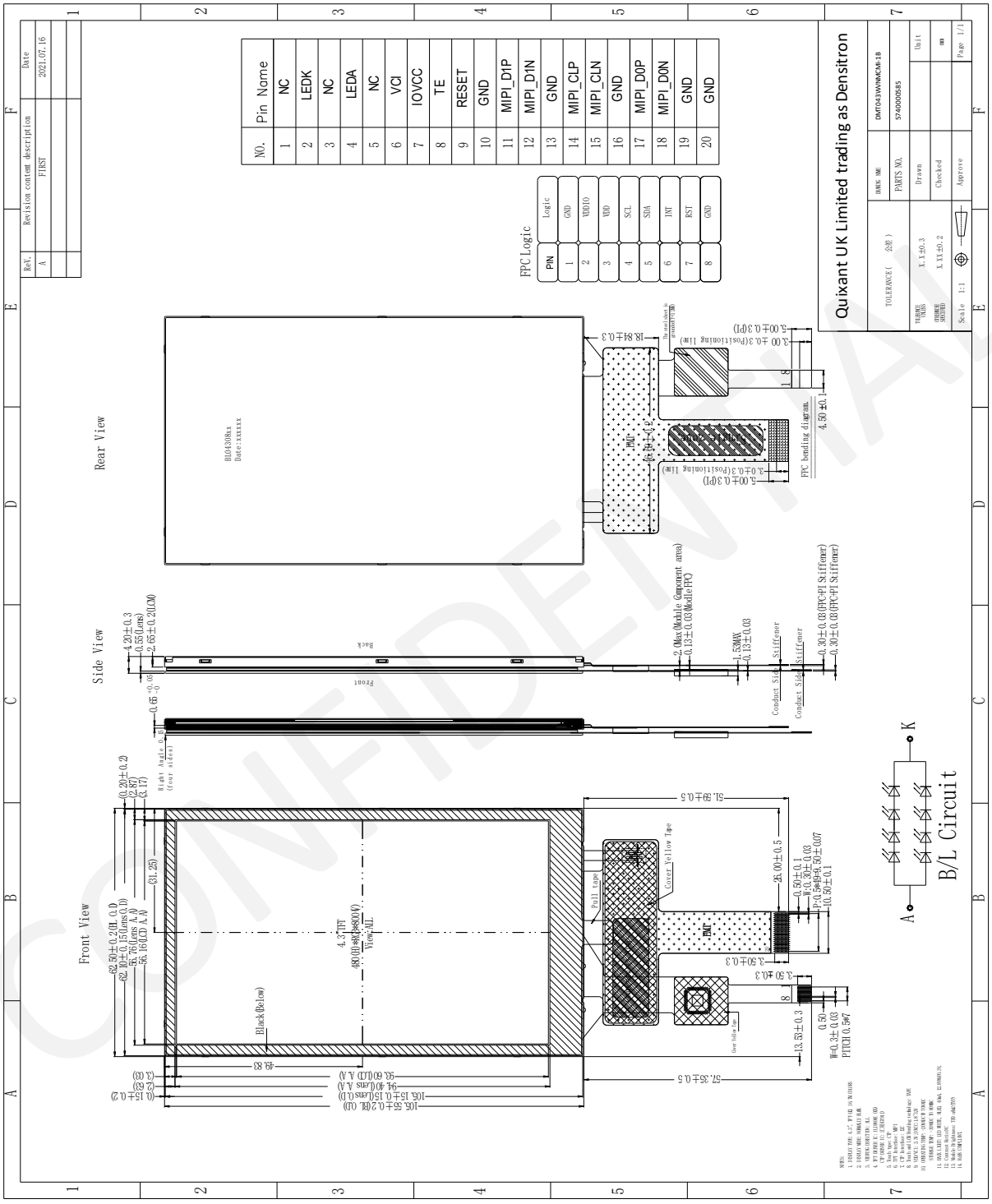
Item	Contents
Touch Structure	G+G
Touch Point	Five points and Gestures
Touch Controller	GT911
Touch Interface	I^2C
Slave Address	0x5D(7bit) or 0x14(7bit)

2. Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Display Format	800 x RGB x 480	Dots
Overall Dimensions	62.50 (H) x 105.55 (V) x 4.20 (D)	mm
Active Area	56.16 (H) x 93.60 (V)	mm
Dot Pitch	0.117 x 0.117	mm
Weight	TBD	g
IC Controller/Driver	ILI9806E	

2.2 Mechanical Drawing



3. Electrical Specification

3.1 Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Note
Digital Supply Voltage	VCI	-0.3	4.6	V	1
Digital Interface Supply Voltage	VDDIO	-0.3	4.6	-	-
Operating Temperature	T_{OP}	-20	+70	°C	-
Storage Temperature	T_{ST}	-30	+80	°C	-

Note 1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

3.2 DC Electrical Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.6	V	-
Digital Interface Supple Voltage	VDDIO	1.65	1.8	3.6	-	-
Normal Mode Current	ICC	-	30	60	mA	-
Level Input Voltage	V_{IH}	$0.7V_{DDIO}$	-	VDDIO	V	-
	V_{IL}	GND	-	$0.3V_{DDIO}$	V	-
Level Output Voltage	V_{OH}	0.8*VDDIO	-	VDDIO	V	-
	V_{OL}	GND	-	0.2*VDDIO	V	-

3.3 Interface Pin Assignment

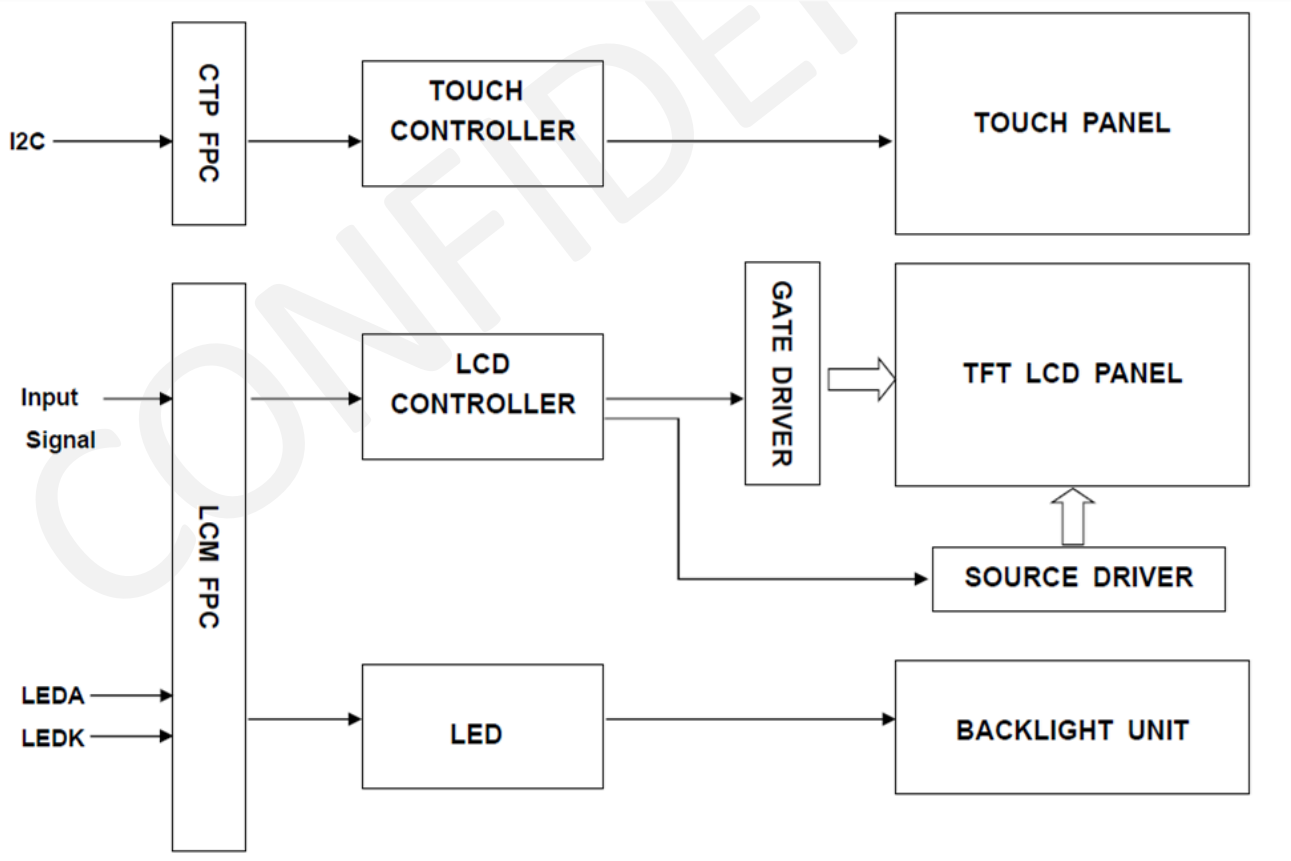
3.3.1 TFT Pin Define

No.	Symbol	I/O	Function
1	NC	-	-
2	LEDK	P	Cathode pin of backlight
3	NC	-	-
4	LEDA	P	Andoe pin of backlight
5	NC	-	-
6	VCI	P	Supply Voltage (3.3V)
7	IOVCC	P	I/O power supply voltage
8	TE	O	Tearing effect output Leave the pin to open when not in use.
9	RESET	I	The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power
10	GND	P	Ground
11	MIPI_D1P	I/O	MIPI DSI differential data pair (DSI-Dn+/-). If MIPI are not used, they should be connected to DGND
12	MIPI_D1N	I/O	
13	GND	P	Ground
14	MIPI_CLP	I	MIPI DSI differential clock pair (DSI-CLK+/-). If MIPI are not used, they should be connected to DGND.
15	MIPI_CLN	I	
16	GND	P	Ground
17	MIPI_D0P	I/O	MIPI DSI differential data pair (DSI-Dn+/-). If MIPI are not used, they should be connected to DGND
18	MIPI_D0N	I/O	
19	GND	P	Ground
20	GND	P	Ground

3.3.2 CTP PIN Assignment

No.	Symbol	I/O	Function
1	GND	P	Ground
2	VDDIO	-	I/O Power Supply Voltage
3	VDD	P	Supply Voltage
4	SCL	I	I2C Clock Input
5	SDA	I	I2C Data Input and Output
6	INT	I	External Interrupt to the Host
7	RST	I	External Reset, Low is Active
8	FND	P	Ground

3.4 Block Diagram



3.5 Timing Characteristics

3.5.1 High Speed Mode – Clock Channel Timing

Figure: DSI Clock Channel Timing

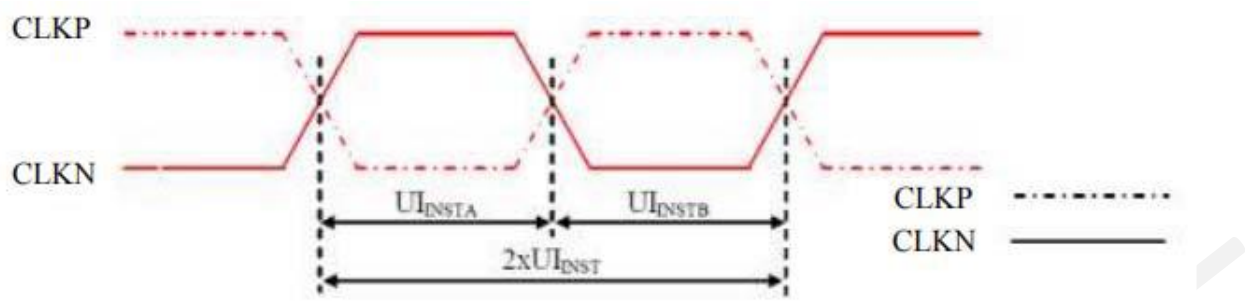


Table: DSI Clock Channel Timing

Signal	Symbol	Item	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	Note 2	12.5	ns

Note 1: UI=UIINSTA=UIINSTB

Note 2: Define the minimum value, see table below.

Table: Limited Clock Channel Speed

Data Type	Two Lanes Speed	Three Lanes Speed	Four Lanes Speed
Data Type=001110 (0Eh), RGB 565, 16UI per pixel	566 Mbps	466 Mbps	366 Mbps
Data Type=011110 (1Eh), RGB 666, 18UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type=10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type=11 1110 (3Eh), RGB 888, 34 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

3.5.2 High Speed Mode - Data Clock Channel Timing

Figure: DSI Data to Clock Channel TImings

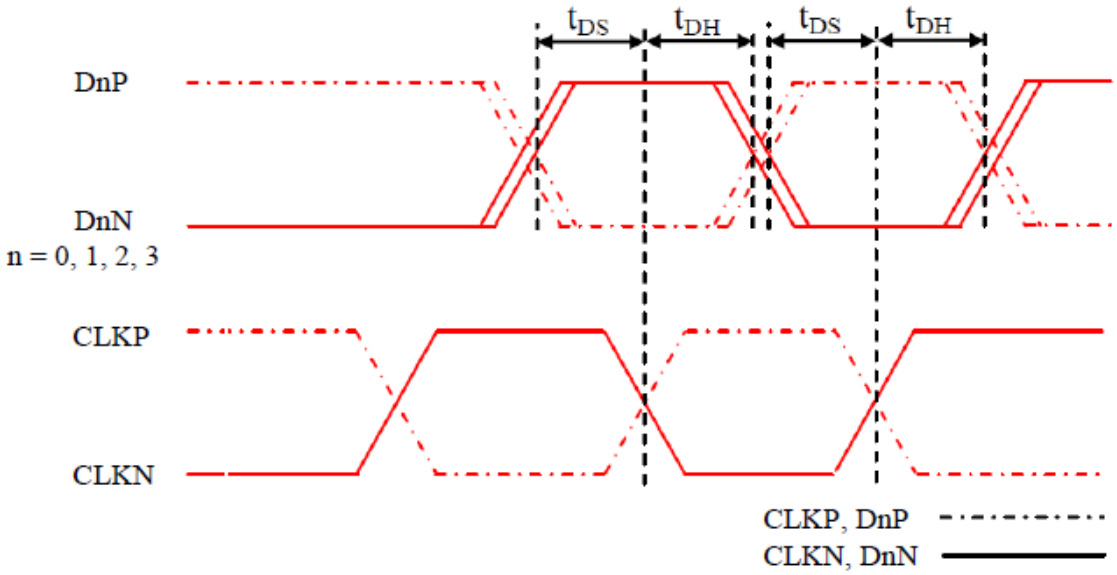


Table: DSI Data to Clock Channel Timings

Signal	Symbol	Item	Min	Max
DnP/N, n=0 and 1	tDS	Data to Clock Setup Time	0.15xUI	-
	tDH	Clock to Data Hold Time	0.15xUI	-

3.5.3 High Speed Mode - Rising and Fall Timings

Figure: Rising and Falling Timings on Clock and Data Channels

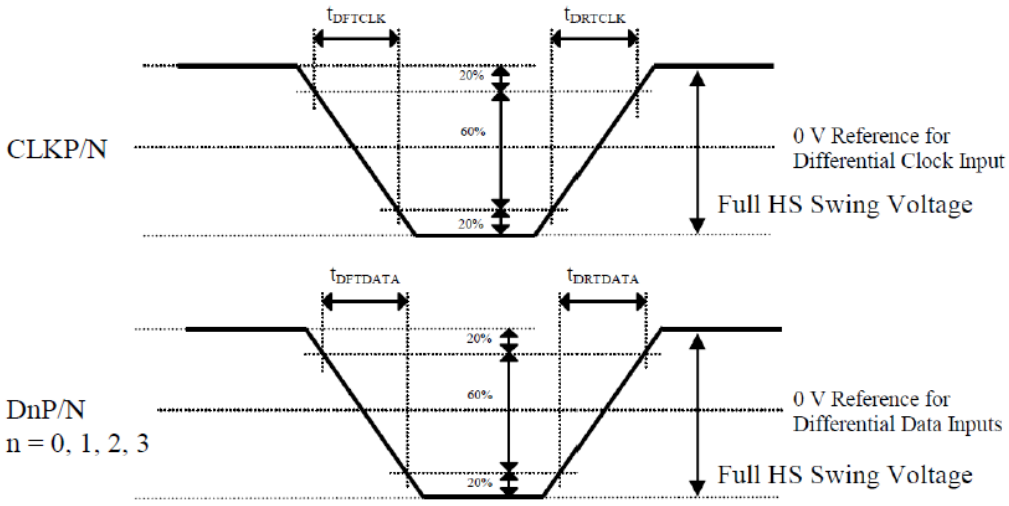


Table: Rise and Fall Timings on Clock and Data Channels

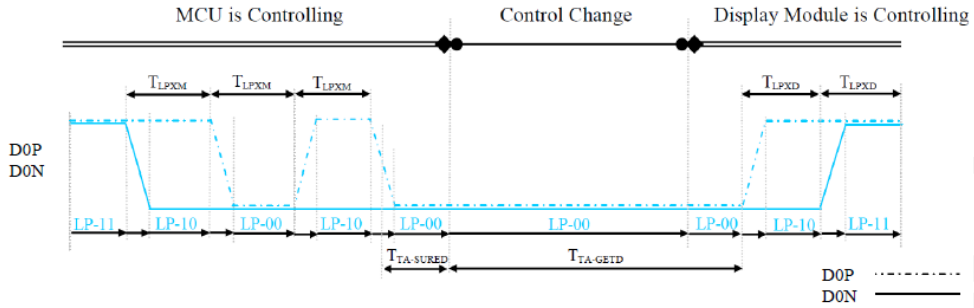
Item	Symbol	Condition	Min	Typ.	Max
Differential Rise Time for Clock	tDRTCLK	CLKP/N	150 ps	-	0.3UI (Note 1)
Differential Rise Time for Data	tDRTDATA	DnP/N n=0 and 1	150 ps	-	0.3UI (Note 1)
Differential Fall Time for Clock	tDFTCLK	CLKP/N	150 ps	-	0.3UI (Note 1)
Differential Fall Time for Data	tDFTDATA	DnP/N n=0 and 1	150 ps	-	0.3UI (Note 1)

Note 1: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

3.5.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

Figure: BTA from the MCU to the Display Module



Lower Power Mode and its State periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

Figure: BTA from the Display Module to the MCU

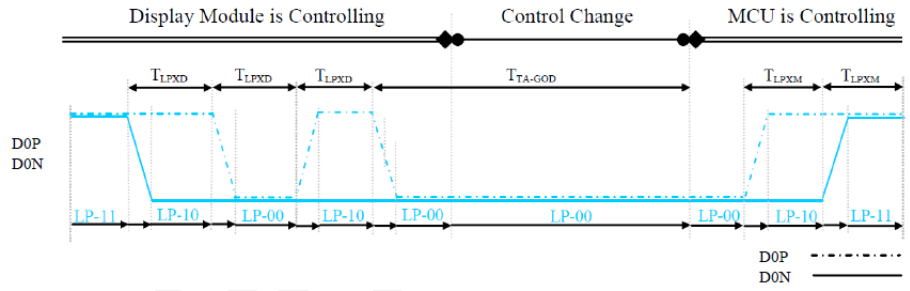


Table: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU→Display Module (ILI9881C)	50	75	ns
D0P/N	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C)→MCU	50	75	ns
D0P/N	TTA-SURED	Time-out before the Display Module (ILI9881C) starts driving	TLPXD	2xTLPXD	ns

Table: Low Power State Period Timings – B

Signal	Symbol	Description	Max	Unit
D0P/N	TTA-GATED	Time to drive LP-00by Display Module (ILI9881C)	5xTLPXD	ns
D0P/N	TTA-GOD	Time to drive LP-00 after turnaround request-MCU	4xTLPXD	ns

3.5.5 Data Lanes from Low Power Mode to High Speed Mode

Figure: Data Lanes-Low Power Mode to High Speed Mode Timings

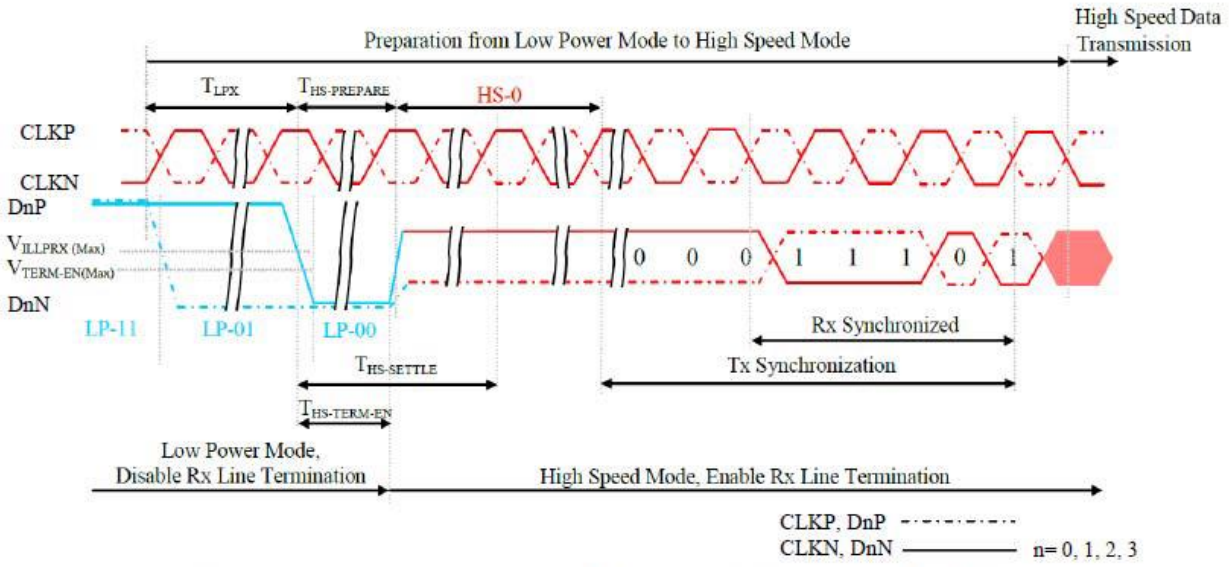


Table: Data Lanes-Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n=0 and 1	TLPX	Length of any Low Power State Period	50	-	ns
DnP/N, n=0 and 1	THS-PREPARE	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n=0 and 1	THS-TERM-EN	Time to enable Data Lane Receiver line termination measured drom when Dn crosses VILMAX	-	35+4xUI	ns

3.5.6 Data Lanes from High Power Mode to High Speed Mode

Figure: Data Lanes-High Speed Mode to Low Power Mode Timings

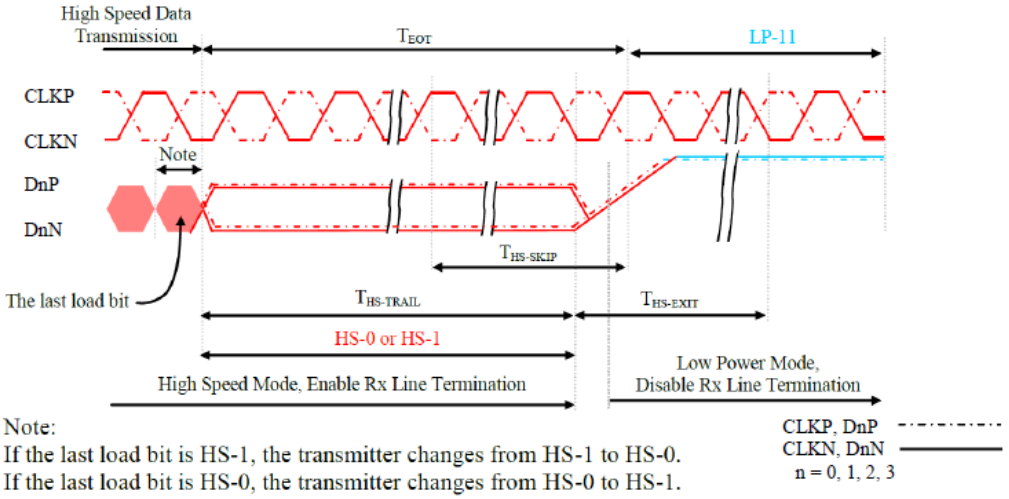


Table: Data Lanes-High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n=0 and 1	THS-SKIP	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n=0 and 1	THS-EXIT	Time to driver LP-11 after HS burst	100	-	ns

3.5.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

Figure: Clock lanes-High Speed Mode to/from Low Power Mode Timings

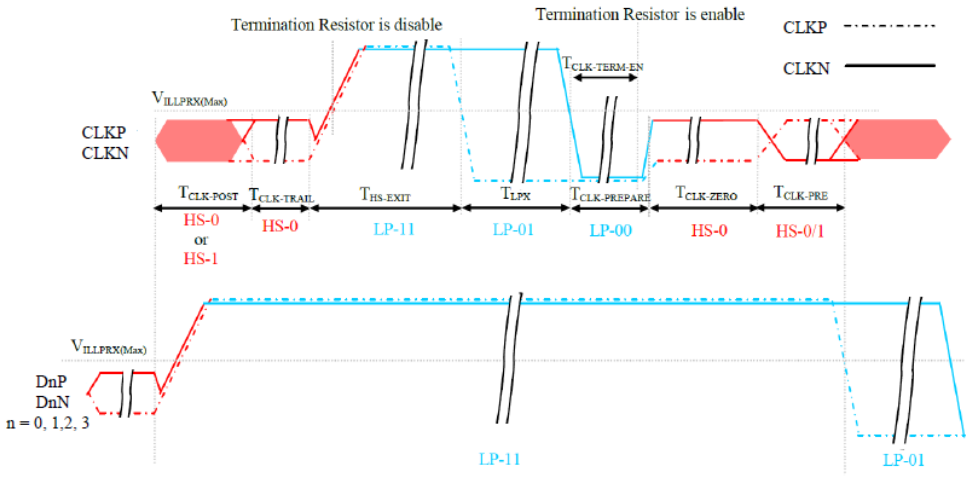


Table: Clock Lanes- High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	TCLK-POST	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	TCLK-TERM-EN	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

3.5.8 Timing for DSI Video Mode

Item	Symbol	Min	Typ.	Max	Unit
DCLK frequency	FCLK	-	67	-	MHz
Horizontal display area	HDISP	-	800	-	Clock
Horizontal Sync. Width	hpw	1	4	-	Clock
Horizontal Sync. Back Porch	hbp	1	38	-	Clock
Horizontal Sync. Front Porch	hfp	1	16	-	Clock
Vertical display area	VDISP	-	1280	-	Line
Vertical Sync. Width	vs	1	4	-	Line
Vertical Sync. Back Porch	vbp	1	10	-	Line
Vertical Sync. Front Porch	vfp	1	8	-	Line
Frame-Rate	-	-	60	-	Hz

Note: The best frame setting: 2 data lanes: 50~60 Hz / 3 data lanes: 50~70 Hz / 4 data lanes: 50~70 Hz.

3.5.9 Reset Input Timing

Figure: Reset Timing

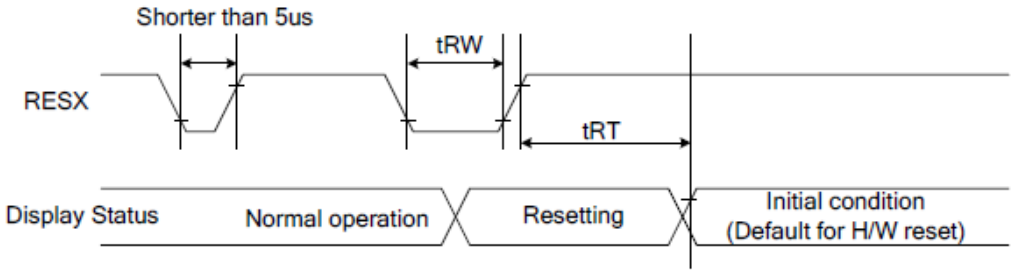


Table: Reset Timing

Signal	Symbol	Item	Min	Max	Unit
RESX	tRW	Reset pulse duration	10	-	us
	tRT	Reset cancel	-	5 (Note 1, 5)	ms
			-	120 (Note 1, 6, 7)	ms

Note 1: The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.

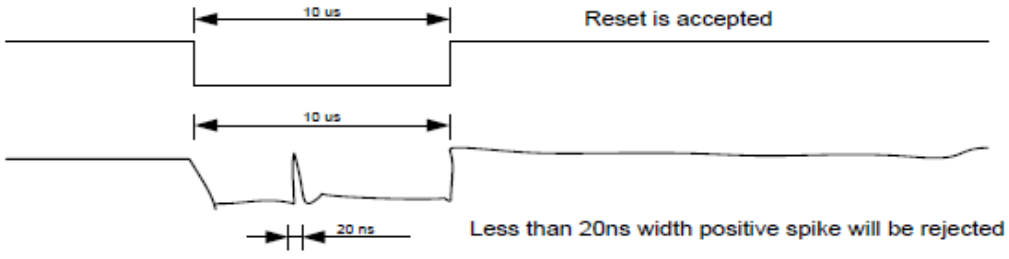
Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

Table: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection can also be applied during a valid reset pulse, as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESC before sending commands. Also Sleep Out command cannot be sent for 120msec.

4. Electrical Specification Touch

4.1 Electrical Characteristics

4.1.1 Absolute Maximum Ratings

Item	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	2.66	-	3.47	V	-
Operating Temperature	T_{OP}	-20	-	+70	℃	-
Storage Temperature	T_{ST}	-30	-	+80	℃	-

4.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V or VDDIO=VDD)

Item	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	2.66	3.3	3.47	V	-
Normal Mode Operating Current	-	-	8	14.5	mA	-
Green Mode Operating Current	-	-	3.3	-	mA	-
Sleep Mode Operating Current	-	70	-	120	uA	-
Doze Mode Operating Current	-	-	0.78	-	mA	-
Digital Input Low Voltage	VIL	-0.3	-	0.25*VDD	V	-
Digital Input High Voltage	VIH	0.75*VDD	-	VDD+0.3	V	-
Digital Output Low Voltage	VOL	-	-	0.15*VDD	V	-
Digital Output High Voltage	VOH	0.85*VDD	-	-	V	-

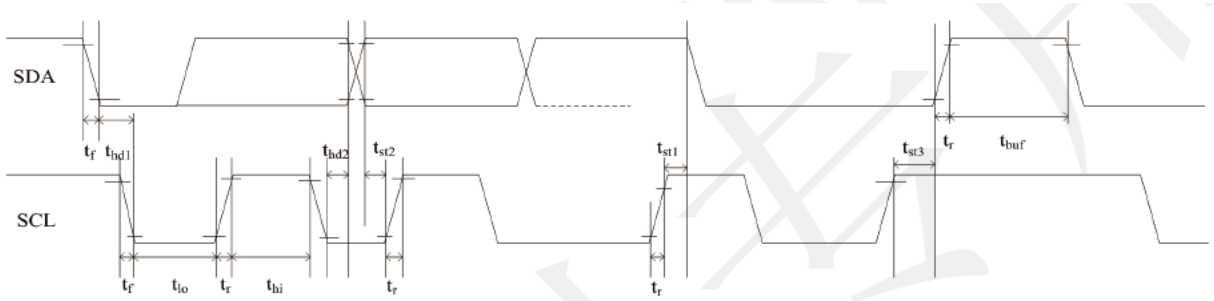
4.1.3 AC Characteristics

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V)

Item	Min	Typ.	Max	Unit	Note
OSC oscillation frequency	59	60	61	MHz	-
I/O output rise time, low to high	-	14	-	ns	-
I/O output rfall time, high to low	-	14	-	ns	-

4.2 I²C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test Condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

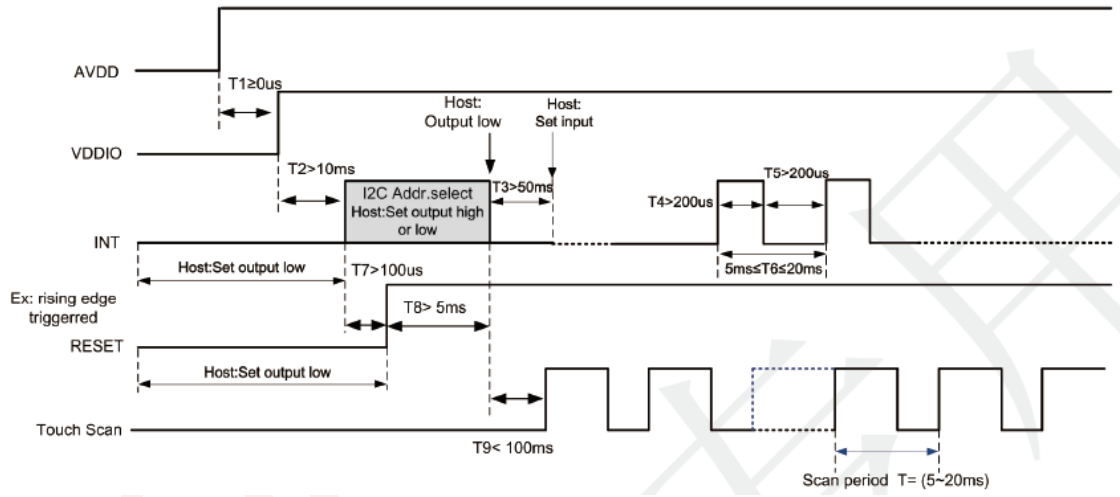
Item	Symbol	Min	Max	Unit
SCL low period	tlo	1.3	-	us
SCL high period	thi	0.6	-	us
SCL setup time for Start condition	tst1	0.6	-	us
SCL setup time for Stop condition	tst3	0.6	-	ns
SCL hold time for Start condition	thd1	0.6	-	us
SDA setup time	tst2	0.1	-	us
SDA hold time	thd2	0	-	us

Test Condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

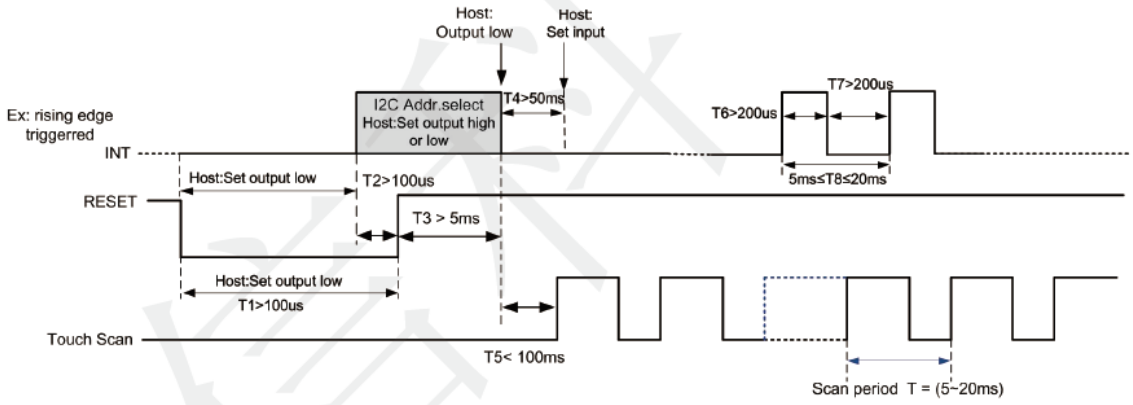
Item	Symbol	Min	Max	Unit
SCL low period	tlo	1.3	-	us
SCL high period	thi	0.6	-	us
SCL setup time for Start condition	tst1	0.6	-	us
SCL setup time for Stop condition	tst3	0.6	-	ns
SCL hold time for Start condition	thd1	0.6	-	us
SDA setup time	tst2	0.1	-	us
SDA hold time	thd2	0	-	us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

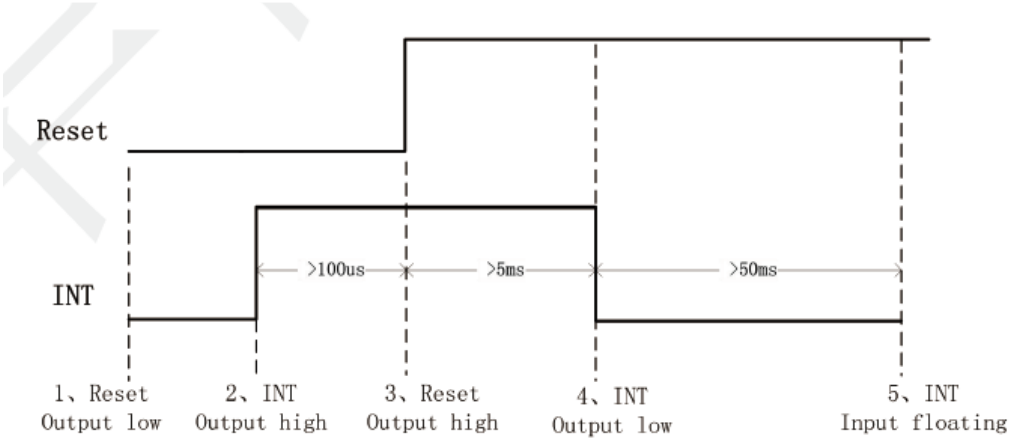
Power-on Timing:



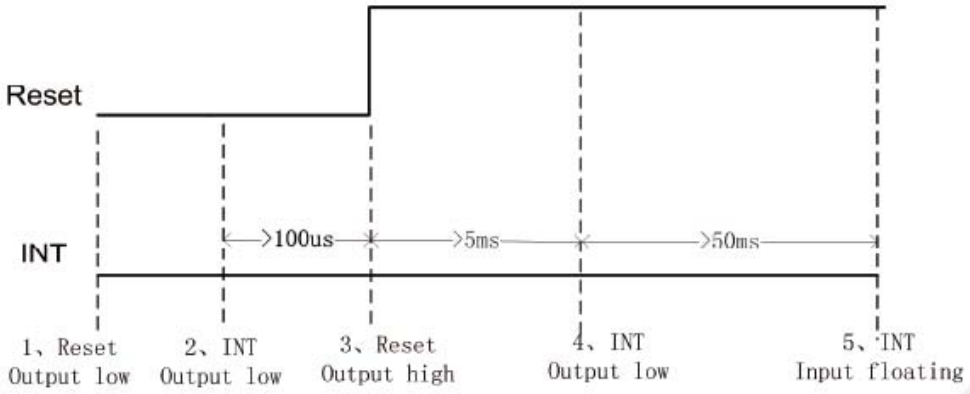
Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



a) Data Transmission

(For example：device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

All slave devices connected to I2C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example：device address is 0xBA/0xBB)

Figure: Timing for Write Operation

The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device. After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example：device address is 0xBA/0xBB)

Figure: Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

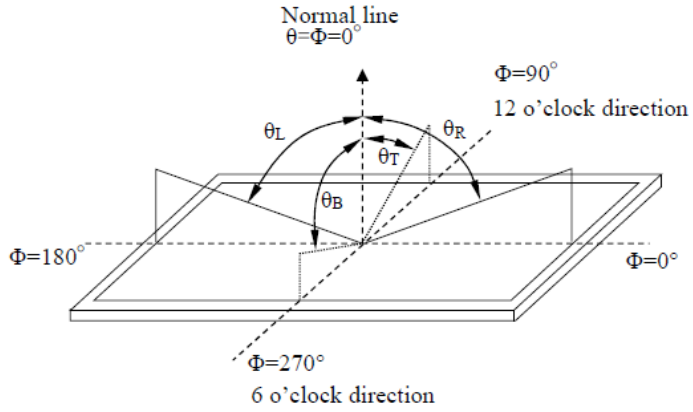
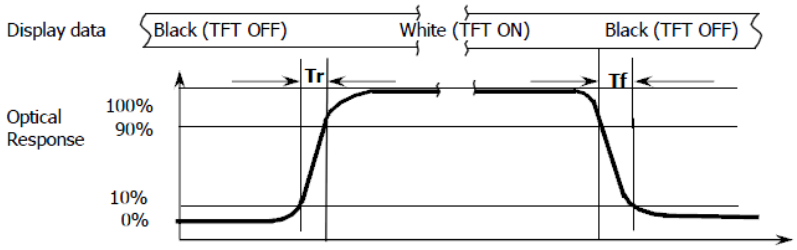
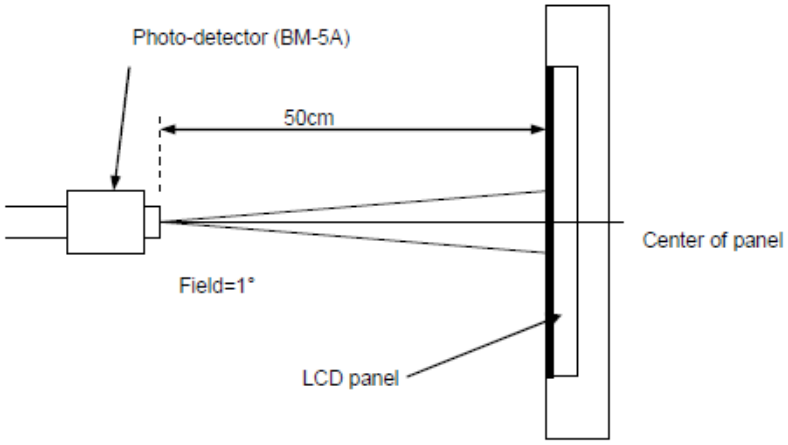
GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

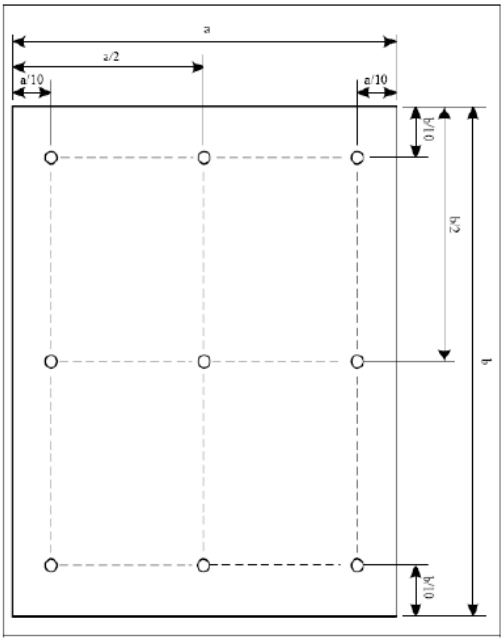
5. Optical Specification

5.1 Optical Characteristics

Characteristics		Symbol	Conditions	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	θ = 0° Normal Viewing Angle	1000	1300	-	-	1, 2
Response time		TR + TF		-	35	40	msec	1, 3
Viewing Angle	Left	θ_x-	CR≥10	70	80	-	-	1, 4
	Right	θ_x+		70	80	-		
	Up	θ_Y+		70	80	-		
	Down	θ_Y-		70	80	-		
Colour Chromaticity	Red	Rx	θ = 0° Normal Viewing Angle	0.5956	0.6356	0.6756	-	1, 4 CF glass
		Ry		0.3113	0.3513	0.3913		
	Green	Gx		0.2720	0.3120	0.3520		
		Gy		0.5324	0.5724	0.6124		
	Blue	Bx		0.1042	0.1442	0.1842		
		By		0.0219	0.0619	0.0659		
	White	Wx		0.2746	0.3146	0.3546		
		Wy		0.3208	0.3608	0.4008		
Luminance		LV	I_F = 20mA	360	405	-	cd/m^2	5
Uniformity		Avg	-	80	-	-	%	5

Measuring Condition: in dark room, at ambient temperature = 25±2°C, 15 min. warm-up time

Note	Item	Test method
1	Definition of Viewing Angle	
2	Definition of Contrast Ratio (CR)	Measured at the center point of panel Contrast ratio (CR) = Luminance measured when LCD is at "white state" / Luminance measured when LCD is at "black state"
3	Definition of Response Time (T_R, T_F)	
4	Definition of Optical Measurement Setup	
5	Definition of Luminance & Uniformity	Luminace Uniformity of these 9 points is defined as below:

Note	Item	Test method
		 $\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$ $\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$

6. LED Backlight Specification

6.1 LED Backlight Characteristics

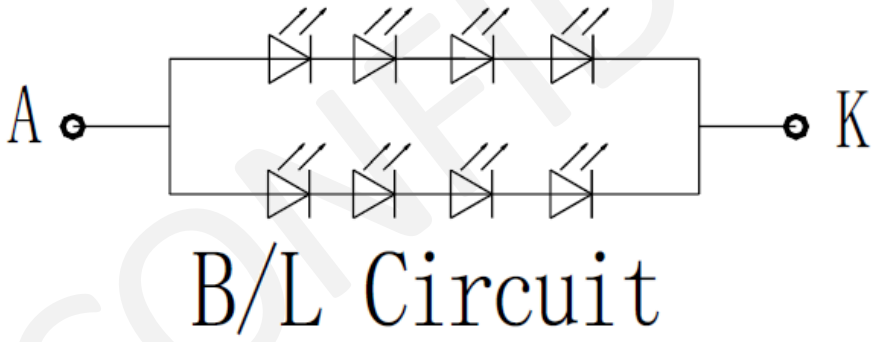
The backlight system is edge-lighting type with 10 chips LED.

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Forward Voltage	Vf	-	-	12.8	-	V	-
Forward Current	If	-	35	40	-	mA	-
LED Life Time	Hr	-	50000	-	-	Hour	1, 2

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.

6.2 INTERNAL CIRCUIT DIAGRAM



7. Packaging

TBD

8. Quality Assurance Specification

8.1 Conformity

The performance, function and reliability of the shipped products conform to the Product Specification.

8.2 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	25 ± 5 C
Humidity:	65% ± 10% RH
Viewing Angle:	Normal Viewing Angle
Illumination:	Single fluorescent lamp (300 to 700Lux)
Viewing distance:	30-50 cm

Finger glove (or finger cover) must be worn by the inspector.

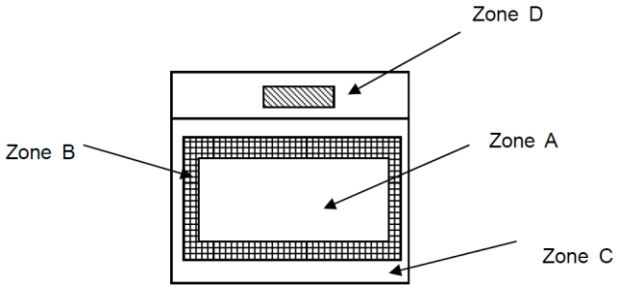
Inspection table or jig must be anti-electrostatic.

8.3 Delivery Assurance

8.3.1 Delivery Inspection Standards

Class II, Normal Inspection, MIL-STD-105E

8.3.2 Zone Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A + Zone B) Area which cannot be seen after assembly by customer.

Zone D: IC Bonding Area

Note: Generally, visual defects in Zone C can be ignored when it doesn't affect product function or appearance after assembly by customer

8.3.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.5	Defects in Cosmetic Check (Display Off)

LCD: Liquid Crystal Display, TP: Touch Panel, LCM: Liquid Crystal Module

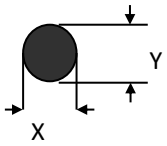
No.	Items	Criteria	Classification of defects
1	Functional defects	1) No display, open or miss line 2) Display abnormally 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Colour tone	Colour unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot, Dim spot, Polarizer Bubble; Polarizer accidented spot.	
6	Soldering Appearance	Good soldering, peeling off is not allowed.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

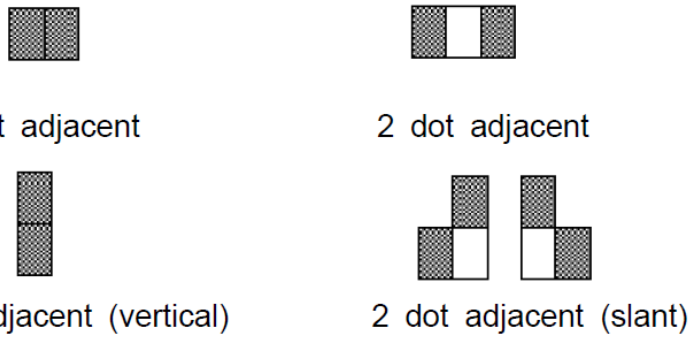
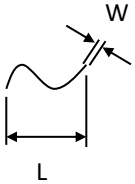
8.3.4 Packing Inspection

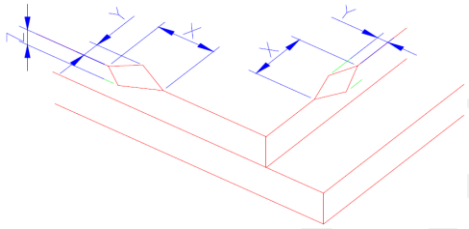
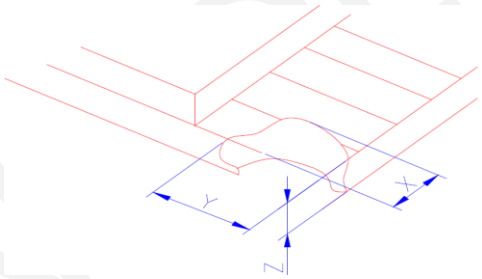
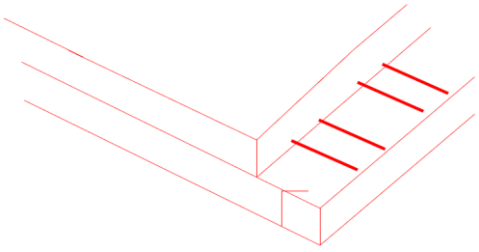
Standard of appearance test for Ⅰ area: (unit: mm)

Note: Defect ignore for Ⅱ area.

8.3.5 Criteria & Classification

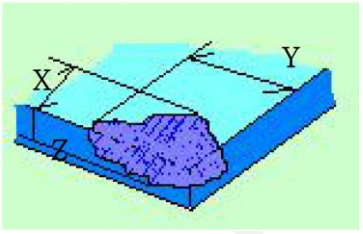
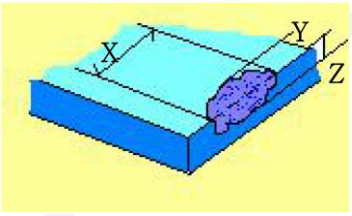
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td rowspan="30">2.0</td><td rowspan="30">Spot Defect</td><td>Round type: as per following drawing, ∅ = (X+Y)/2  </td></tr>
<tr><td>1) Light Dot (Black/white spot, pinhole, stain)</td></tr>
<tr><td>Size\Zone | Acceptable Quantity
A | B | C
∅≤0.15 | Ignore | Ignore
0.15<∅≤0.25 | 3 (distance ≧ 10mm) | Ignore
0.25<∅≤0.40 | 2 (distance ≧ 10mm) | Ignore
0.40<∅ | 0 | Ignore</td></tr>
<tr><td>2) Dim Spot (Light leakage, dent, dark spot)</td></tr>
<tr><td>Size\Zone | Acceptable Quantity
A | B | C
∅≤0.15 | Ignore | Ignore
0.15<∅≤0.25 | 3 (distance ≧ 10mm) | Ignore
0.25<∅≤0.40 | 2 (distance ≧ 10mm) | Ignore
0.40<∅ | 0 | Ignore</td></tr>
<tr><td>3) Polarizer Accidented Spot</td></tr>
<tr><td>Size\Zone | Acceptable Quantity
A | B | C
∅≤0.2 | Ignore | Ignore
0.2<∅≤0.5 | 2 (distance ≧ 10mm) | Ignore
0.5<∅ | 0 | Ignore</td></tr>
<tr><td>4) Pixel Bad Points</td></tr>
<tr><td>Item | Zone A | Acceptable Quantity
Bright dot | Random | N≤2
2 dots adjacent | N≤0
3 dots adjacent | N≤0
Dark dot | Random | N≤2
2 dots adjacent | N≤0</td></tr>
</table>

<table>
<tr><th>Class</th><th>Item</th><th colspan="4">Criteria</th></tr>
<tr><td rowspan="11"></td><td rowspan="11"></td><td></td><td>3 dots adjacent</td><td colspan="2">N≤0</td></tr>
<tr><td>Distance</td><td>1. Minimum Distance Between Bright dots.
2. Minimum Distance Between dark dots
3. Minimum Distance Between dark and bright dot.</td><td colspan="2">5mm</td></tr>
<tr><td colspan="2">Total bright and dark dot</td><td colspan="2">N≤4</td></tr>
<tr><td colspan="5">Note:
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.
C) 2 dot adjacent = 1 pair = 2 dots
Picture:
 
2 dot adjacent
2 dot adjacent
2 dot adjacent (vertical)
2 dot adjacent (slant)</td></tr>
<tr><td colspan="5">5) Polarizer Bubble</td></tr>
<tr><td rowspan="2">Size\Zone</td><td colspan="3">Acceptable Quantity</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>∅≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.2<∅≤0.4</td><td colspan="2">3 (distance ≧ 10mm)</td></tr>
<tr><td>0.4<∅</td><td colspan="2">0</td></tr>
<tr><td rowspan="3">3.0</td><td rowspan="3">Line Defect (LCD/TP/ Polarizer backlight black/white line,</td><td colspan="4">Line type: as per following drawing
 
</td></tr>
<tr><td></td><td>Length</td><td colspan="2">Acceptable quantity</td></tr>
</table>

<table>
<tr><th>Class</th><th>Item</th><th colspan="5">Criteria</th></tr>
<tr><td rowspan="5"></td><td rowspan="5">scratch, stain)</td><td>Width</td><td></td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>W≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L ≤ 4.0</td><td colspan="2">N ≤ 3</td></tr>
<tr><td>0.06<W≤0.08</td><td>L ≤ 3.0</td><td colspan="2">N ≤ 2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
<tr><td>1.0</td><td>LCD
Crack/Broken</td><td colspan="5">Symbols:
X: Length, Y: Width, Z: Height, L: Length of ITO, T: Height of LCD
1) The edge of LCD broken: X≦3.0mm; Y<Inner border line of the seal; Z≦T
 
2) LCD corner broken: X≦3.0mm; Y≦L; Z≦T
  </td></tr>
<tr><td>Major</td><td>LCD Crack</td><td colspan="5">The LCD with extensive crack is not acceptable.
  </td></tr>
<tr><td>4.0</td><td>Electronic
Components
SMT</td><td colspan="5">Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite</td></tr>
</table>

Class	Item	Criteria
5.0	Display colour & Brightness	1) Colour: Measuring the colour coordinates in accordance with the datasheet or samples. 2) Brightness: Measuring the brightness of white screen in accordance with the datasheet or samples.
6.0	LCD Mura	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.

Class	Item	Criteria				
7.0	CTP Related	1) CTP Cover Sensor Accidented Black/White Spot				
		Size\Zone	Acceptable Qty			
			A	B	C	
		∅≤0.1	Ignore		Ignore	
		0.1<∅≤0.2	3（distance≧10mm）			
		0.20<∅≤0.25	2			
		0.3<∅	0			
		2) CTP Cover Scratch				
		Width	Length	Acceptable Qty		
				A	B	C
		Φ≤0.05	Ignore	Ignore		
		0.05<W≤0.06	L≤4.0	N≤3		
		0.07<W≤0.08	L≤3.0	N≤2		
		0.08<W	Define as spot defect			
		3) CTP Cover Pinhole / Lack of ink				
		Size\Zone	Acceptable Qty			
			C			
		∅≤0.1	Ignore			
		0.1<∅≤0.2	3 (distance ≧ 10mm)			
		0.25<∅≤0.3	2			
		0.35<∅	0			
		4) CTP Bonding Bubble / Accidented Spot				
		Size\Zone	Acceptable Qty			
			A	B		
		∅≤0.1	Ignore			
		0.15<∅≤0.20	3 (distance≧10mm）			

Class	Item	Criteria	
		0.20<∅≤0.25	2
		0.25<∅	0
		Assembly Deflection: beyond the edge of backlight ≤0.2mm	
Minor	CTP Related	TP cover broken X: length, Y: width, Z: height X≤0.5mm; Y≤0.5mm; Z<Cover thickness *Circuitry broken is not allowed.	
		TP cover broken X: length, Y: width, Z: height X≤0.3mm; Y≤0.3mm; Z<LCD thickness *Circuitry broken is not allowed.	

Criteria (functional items)

No.	Item	Criteria
1	No display	Not allowed
2	Missing segment	
3	Short	
4	Backlight no lighting	
5	TP no function	

8.4 Dealing with Customer Complaints

8.4.1 Non-conforming Analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.

After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

8.4.2 Handling of Non-conforming Displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

9. Reliability Specification

9.1 Reliability Tests

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Non-display; 3. Missing segments/line; 4. Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operation	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10℃,30 min ↔ 60℃,30 min, Change time:5min 20CYC.	
ESD Test	C=150pF, R=330, 5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm (MEDIUM BOX)	

Note 1: The test samples should be applied to only one test item.
Note 2: Sample size for each test item is 5~10pcs.
Note 3: For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.
Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
Note 5: Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
Note 6: The color fading mura of polarizing filter should not care.

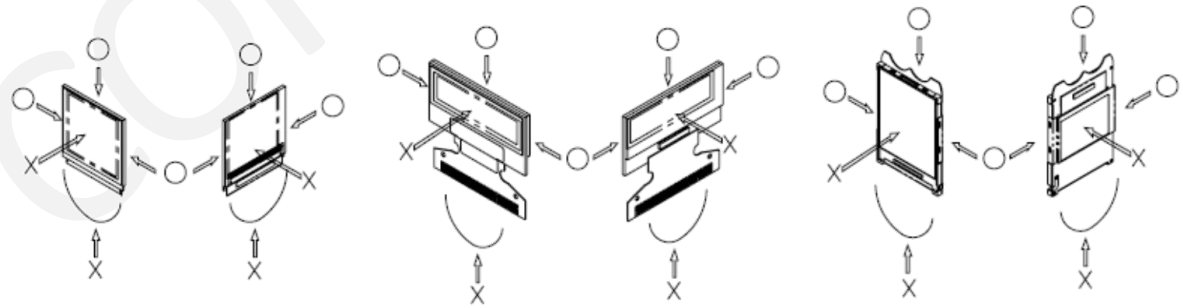
9.1.1 Inspection Check Standard

After the completion of the described reliability test, the samples are to be left at room temperature for 4 hrs prior to conducting the inspection check at 25±5 °C, 65±10% RH.

10. Handling Precautions

10.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water
4) If pressure is applied to the display surface or its neighbourhood of the display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
5) The polarizer covering the surface of the display module is soft and easily scratched. Please be careful when handling the display module.
6) When the surface of the polarizer of the display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   a. Scotch Mending Tape No. 810 or an equivalent
   b. Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   c. Also, pay attention that the following liquid and solvent may spoil the polarizer:
      - Water
      - Ketone
      - Aromatic Solvents
7) Hold the display module very carefully when placing it into the system housing. Do not apply excessive stress or pressure to display module. And, do not over bend the film with electrode pattern layouts. These stresses will



influence the display performance. Also, secure sufficient rigidity for the outer cases.
8) Do not apply stress to the LSI chips and the surrounding molded sections.
9) Do not disassemble nor modify the display module.
10) Do not apply input signals while the logic power is off.
11) Pay sufficient attention to the working environments when handing display modules to prevent occurrence of element breakage accidents by static electricity.

a. Be sure to make human body grounding when handling display modules.
b. Be sure to ground tools to use or assembly such as soldering irons.
c. To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
d. Protective film is being applied to the surface of the display panel of the display module. Be careful since static electricity may be generated when exfoliating the protective film.

12) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. If the display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
13) If electric current is applied when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

10.2 Storage Precautions

1) When storing display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the display module, when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

10.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the display module, fasten the external plastic housing section.
7) If power supply to the display module is forcibly shut down by such errors as taking out the main battery while the display panel is in operation, we cannot guarantee the quality of this display module.

10.4 Operation Precautions

1) It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.
2) Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation.
3) Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged.
4) To protect display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the display modules.
   a. Pins and electrodes
   b. Pattern layouts such as the FPC
5) When the driver is being exposed (COG), semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if the driver is exposed to light, malfunctioning may occur.
   a. Design the product and installation method so that the driver may be shielded from light in actual usage.
   b. Design the product and installation method so that the driver may be shielded from light during the inspection processes.
6) Although the display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
7) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

10.5 Other Precautions

1) Request the qualified companies to handle industrial wastes when disposing of the display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.