Amendment history of SSD1351 Specification

Revision	Description of any change	Issued	Effective
0.10 C6FA1 30-May-08	1st draft Approver list: Product Marketing- Raymond Ho Design Engineering- Kenneth Lee Product Engineering- Jimmy Chiu Quality & Manufacturing-Daniel Ho Test Engineering - Warren Wong	Johnkid Lo	10-Jun-08
1.0 C6FA2 11-Dec-08	1. Change to Advance information 2. Add amendment history 3. Add U1 , U2, U3 dwg into appendix 4. Revise die thickness tolerance from ±25um to ±15um on Fig 5-1 & section 3 5. Remove "The typical regulated V_{DD} is about 2.5V" in section 8.10 & figure 14-1 6. Revise table 12-1 DC characteristic 7. Revise table 13-1,13-2,13-3,13-4,13-5 (V_{CI} range) AC characteristic 8. Remove V_{DD} range in Section 12 &13 9. Revise command table for A0h, 96h, B2h 10. Revise V_{CC} voltage range from 10V-20V to 10V to 18V i. Section 2 Feature list ii. Section 8.6 SEG/COM Driving block iii. Section 11 Maximum rating iv. Section 12 DC characteristic v. Section 14 Application example 11. Revise typo in Table 6-1: SSD1351UR1 Pin Assignment Table Approver list: Product Marketing- Raymond Ho Design Engineering- Kenneth Lee Product Engineering- Johnkid Lo Quality & Manufacturing-Kenneth Ho Test Engineering - Stephen Leung	Ada Ng	12-Dec-08
1.1 C6FA2 19-Feb-09	1 Revised Section 8.1 MCU interface 1.1 Revise Figure 8-2 & 8-3 : from D[7:0] to D[17:0] 1.2 Revise Section 8.1.3 & 8.1.4, Figure 8-5, Figure 8-6, Figure 13-3, Figure 13-4 : From "RW acts as SCLK, D0 acts as SDIN" to "D0 acts as SCLK, D1 acts as SDIN" 2 Revised Note (5) of Figures 8-13 & 8-14 on P.30 3 Add SSD1351U4R1 in appendix. Approver list: Product Marketing- Raymond Ho Design Engineering- Kenneth Lee Product Engineering- Johnkid Lo Quality & Manufacturing-Daniel Ho Test Engineering - Stephen Leung	Ada Ng	20-Feb-09

SSD1351

Advance Information

128 RGB x 128 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

Appendix: IC Revision history of SSD1351 Specification

Version	Change Items	Effective Date
0.10	1. 1st release	10-Jun-08
1.0	1. Change to Advance Info 2. Revise die thickness tolerance from ±25um to ±15um 3. Revise table 12-1 DC characteristic 4. Revise tables 13 AC characteristic 5. Revise command table 6. Revise V_{CC} voltage range	12-Dec-08
1.1	1. Revised section 8.1 MCU interface	20-Feb-09

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

The SSD1351 is a CMOS OLED/PLED driver with 384 segments and 128 commons output, supporting up to 128RGB x 128 dot matrix display. This chip is designed for Common Cathode type OLED/PLED panel.

The SSD1351 has embedded Graphic Display Data RAM (GDDRAM). It supports with 8, 16, 18 bits 8080 / 6800 parallel interface, Serial Peripheral Interface. It has 256-step contrast and 262K color control, giving vivid color display on OLED panels.

2 FEATURES

- Resolution: 128 RGB x 128 dot matrix panel
- 262k color depth supported by embedded 128x128x18 bit SRAM display buffer
- Power supply
  - V_{DD} = 2.4V – 2.6V (Core V_{DD} power supply, can be regulated from V_{CI})
  - V_{DDIO} = 1.65V – V_{CI} (MCU interface logic level)
  - V_{CI} = 2.4V – 3.5V (Low voltage power supply)
  - V_{CC} = 10.0V – 18.0V (Panel driving power supply)
  - When V_{CI} is lower than 2.6V, V_{DD} should be supplied by external power source
- Segment maximum source current: 200uA
- Common maximum sink current: 70mA
- 256 step brightness current control for the each color component plus 16 step master current control
- Pin selectable MCU Interfaces:
  - 8/16/18 bits 6800-series parallel interface
  - 8/16/18 bits 8080-series parallel interface
  - 3 –wire and 4-wire Serial Peripheral Interface
- Support various color depths
  - 262k color (6:6:6)
  - 65k color (5:6:5)
- Gamma Look Up Tables (GLUT) with 8 bit entry
- Row re-mapping and Column re-mapping
- Vertical and horizontal scrolling
- Programmable Frame Rate and Multiplexing Ratio
- On-Chip Oscillator
- Color Swapping Function (RGB – BGR), arranged in RGB sequence when reset
- Slim chip layout for COF
- Operating temperature range -40°C to 85°C.

3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1351Z	128RGB	128	Gold Bump Die	9 , 57	• Min SEG pad pitch: 25um • Min COM pad pitch: 35um • Die thickness : 300 +/- 15um
SSD1351UR1	128RGB	128	COF	12 , 56	• 48mm film, 4 sprocket hole • Hot bar type COF • 8/16/18-bit 80/68/SPI interface • SEG lead pitch: 0.050x0.999=0.04995mm • COM lead pitch: 0.06x0.999=0.05994mm

4 BLOCK DIAGRAM

Figure 4-1 Block Diagram