TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6C03

COLUMN AND ROW DRIVER FOR A DOT MATRIX LCD

The T6C03 is a 160−channel−output column and row driver for an STN dot matrix LCD.
The T6C03 features a 42−V LCD drive voltage and an 8−MHz maximum operating frequency. The T6C03 is able to drive LCD panels with a duty ratio of up to 1 / 480.

Unit: mm

T6C03	LEAD PITCH	
	IN	OUT
(UA)	0.8	0.14

Please contact with Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

Features

- Display duty application : to 1 / 480
- LCD drive signal : 160
- Data transfer : Column: 4 / 8−bit bidirectional
  Row: Single / Dual bidirectional
- Operating frequency : 8 MHz (V_{DD} = 5 V ± 10%)
- LCD drive voltage : 14 to 42 V
- Power supply voltage : 2.7 to 5.5 V
- Operating temperature : −20 to 75°C
- LCD drive output resistance : 1.3 kΩ (max) (20 V, 1 / 13 bias)
- Display−off function : When / DSPOF is L, all LCD drive outputs (O1 to O160) remain at the V5 level.
- Low power consumption : Cascade connection and auto enable transfer functions are available.
- EI / LP input : EI / LP input enables LSI operation.
  Connect EIO1 / 2 from the 1st LSI to L.

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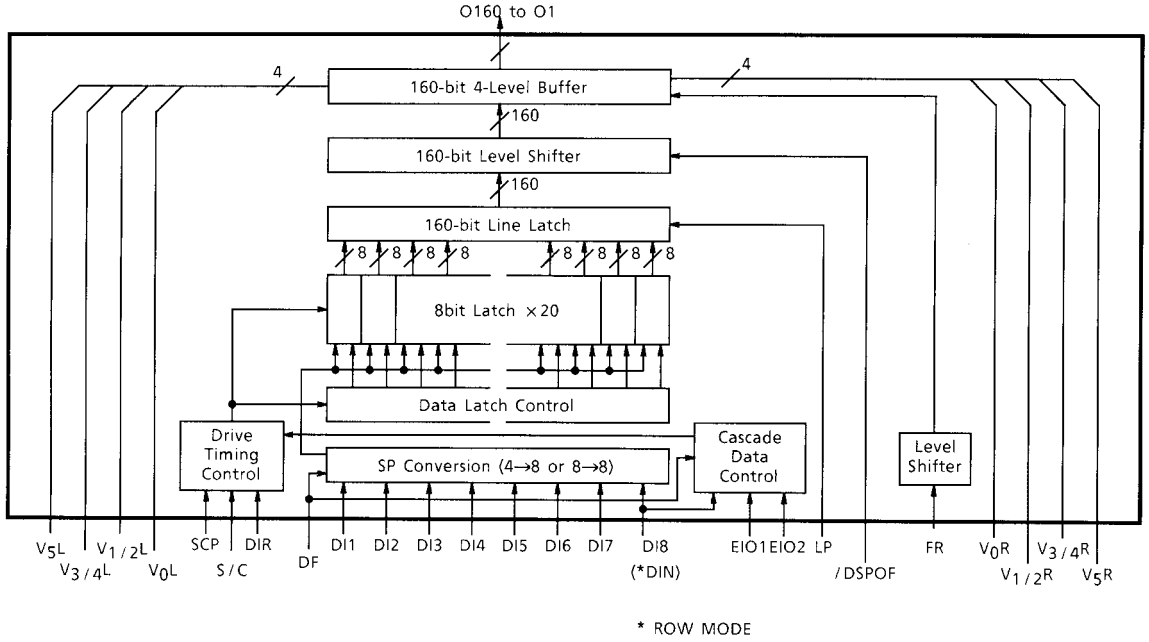
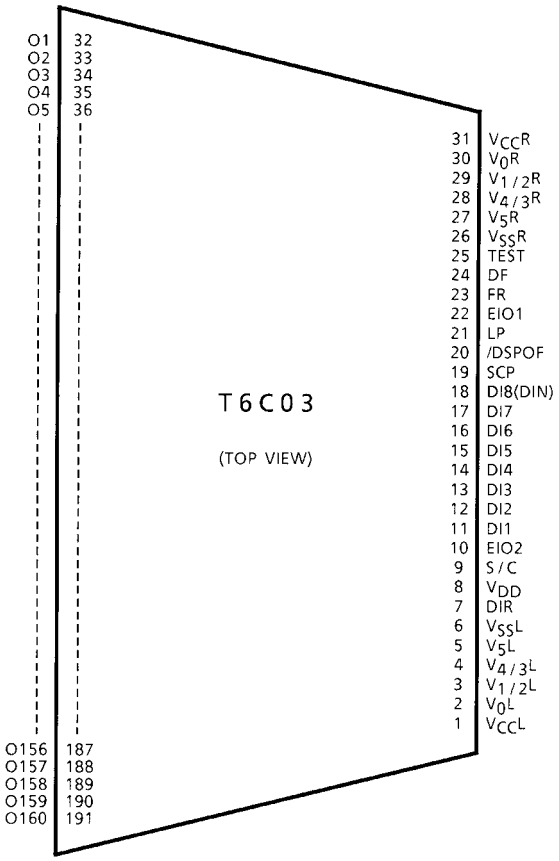
Block Diagram



* ROW MODE

Pin Assignment



Note: The above diagram shows the pin configuration of the LSI Chip, not that of the tape carrier package.

Pin Functions

Pin Name	I / O	Functions	Level
O1 to O160	Output	Output for LCD drive signal	V_0 to V_5
EIO1, EIO2	I / O	(Column mode) Input / output for enable signal DIR selects In or Out. Connect EIO (IN) of 1st LSI to L. For a cascade connection, connect EIO (OUT) to EIO (IN) of next LSI.	V_{DD} to V_{SS}
		(Row mode) Input / output for shift data DIR = L : EIO1 is output, EIO2 is input DIR = H: EIO1 is input, EIO2 is output	
DI1 to DI8	Input	(Column mode) Input for data signal	
		(Row mode) DI1 to DI7: Fix to H or L, DI8: when DF = H, use as DIN	
DIR	Input	(Direction) Input for data flow direction select	
/ DSPOF	Input	(Display off) / DSPOF = L : Display−off mode, (O1 to O160) remain at the V_5 level / DSPOF = H: Display−on mode, (O1 to O160) are operational.	
DF	Input	(Data format) Input for data bit select	
LP	Input	(Latch pulse) Display data is latched on falling edges of LP. When EIO (IN) = L, $\overline{SCP} \cdot LP$ = H enables the 1st LSI.	
		(Row mode) Input for shift clock pulse	
FR	Input	(Frame) Input for frame signal	
SCP	Input	(Column mode) Input for shift clock pulse	
		(Row mode) Fix to H or L	
TEST	Input	(TEST) Fix to L	
S / C	Input	Input for mode select: H = Column mode, L = Row mode	

Pin Name	I / O	Functions	Level
V_{DD}	—	Power supply for internal logic (+5.0 V)	—
V_{SS}	—	Power supply for internal logic (0 V)	
$V_5L \cdot R$	—	Power supply for LCD drive circuit	
$V_{3/4}L \cdot R$	—	Power supply for LCD drive circuit	
$V_{2/1}L \cdot R$	—	Power supply for LCD drive circuit	
$V_0L \cdot R$	—	Power supply for LCD drive circuit	
$V_{CC}L \cdot R$, $V_{SS}L \cdot R$	—	Power supply for LCD drive circuit	

Relation Between FR, Data Input and Output Level

F R	Data Input	/ Dspof	Output Level (Column Mode)	Output Level (Row Mode)
L	L	H	V_3	V_4
L	H	H	V_5	V_0
H	L	H	V_2	V_1
H	H	H	V_0	V_5
(Note)	(Note)	L	V_5	V_5

Note: Don’t Care

Data Input Format

Column Mode

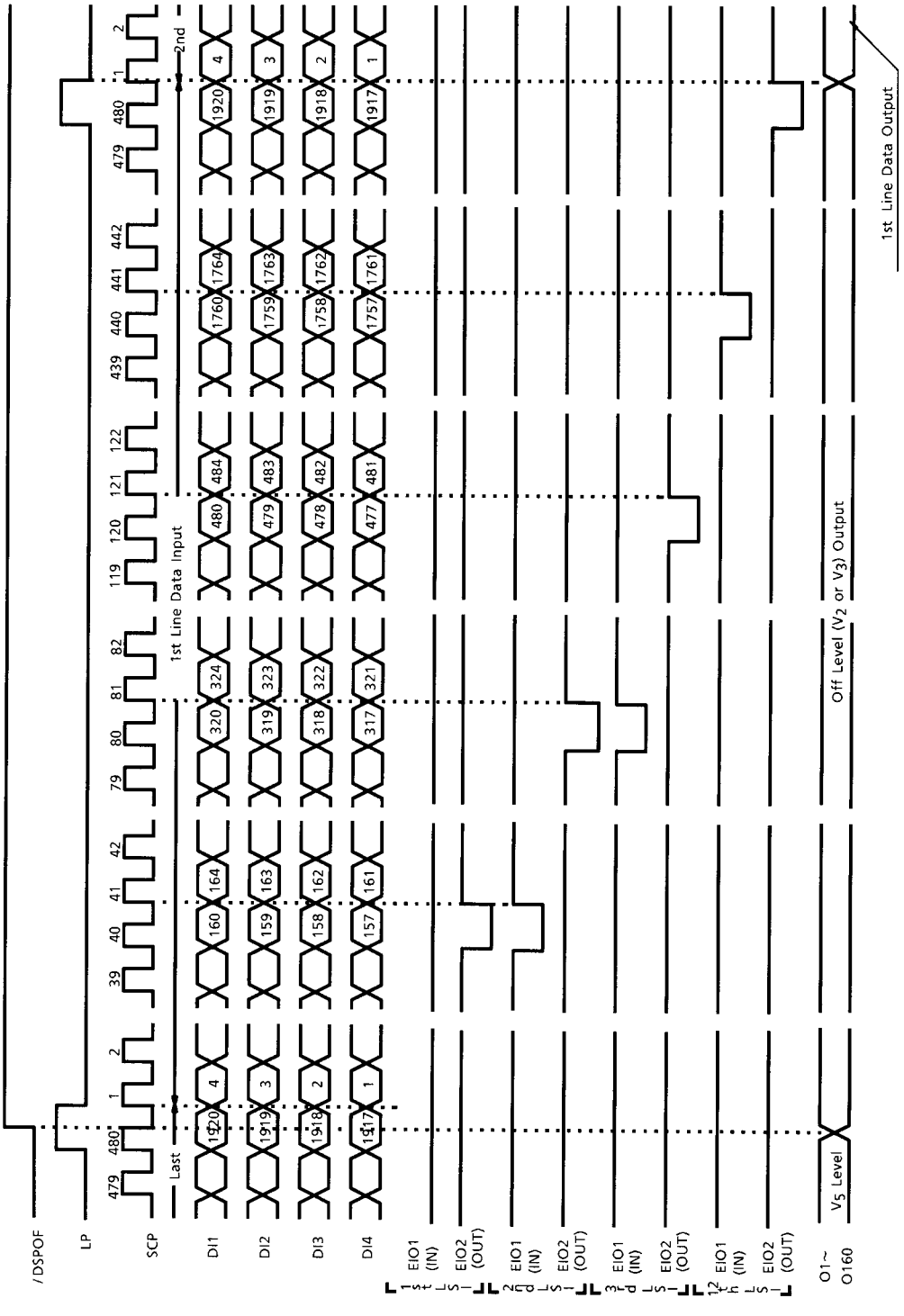
DIR	DF	BIT Mode	Enable Pin		(Note 1)	Input Data Line and Output Buffers							
			EIO1	EIO2		DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8
H	L	4−BIT	IN	OUT	L	O160	O159	O158	O157	—	—	—	—
					F	O4	O3	O2	O1	—	—	—	—
L			OUT	IN	L	O1	O2	O3	O4	—	—	—	—
					F	O157	O158	O159	O160	—	—	—	—
H	H	8−BIT	IN	OUT	L	O160	O159	O158	O157	O156	O155	O154	O153
					F	O8	O7	O6	O5	O4	O3	O2	O1
L			OUT	IN	L	O1	O2	O3	O4	O5	O6	O7	O8
					F	O153	O154	O155	O156	O157	O158	O159	O160

Note 1: L: Last Data
F: First Data

Row Mode

DIR	DF	Data Flow	Data Input Terminals		
			EIO1	EIO2	DIN
L	L	O160 → O1	OUT	IN	—
H		O1 → O160	IN	OUT	—
L	H	O160 → O81 O80 → O1	OUT	IN	IN
H		O1 → O80 O81 → O160	IN	OUT	IN

Timing Diagram (Column mode)



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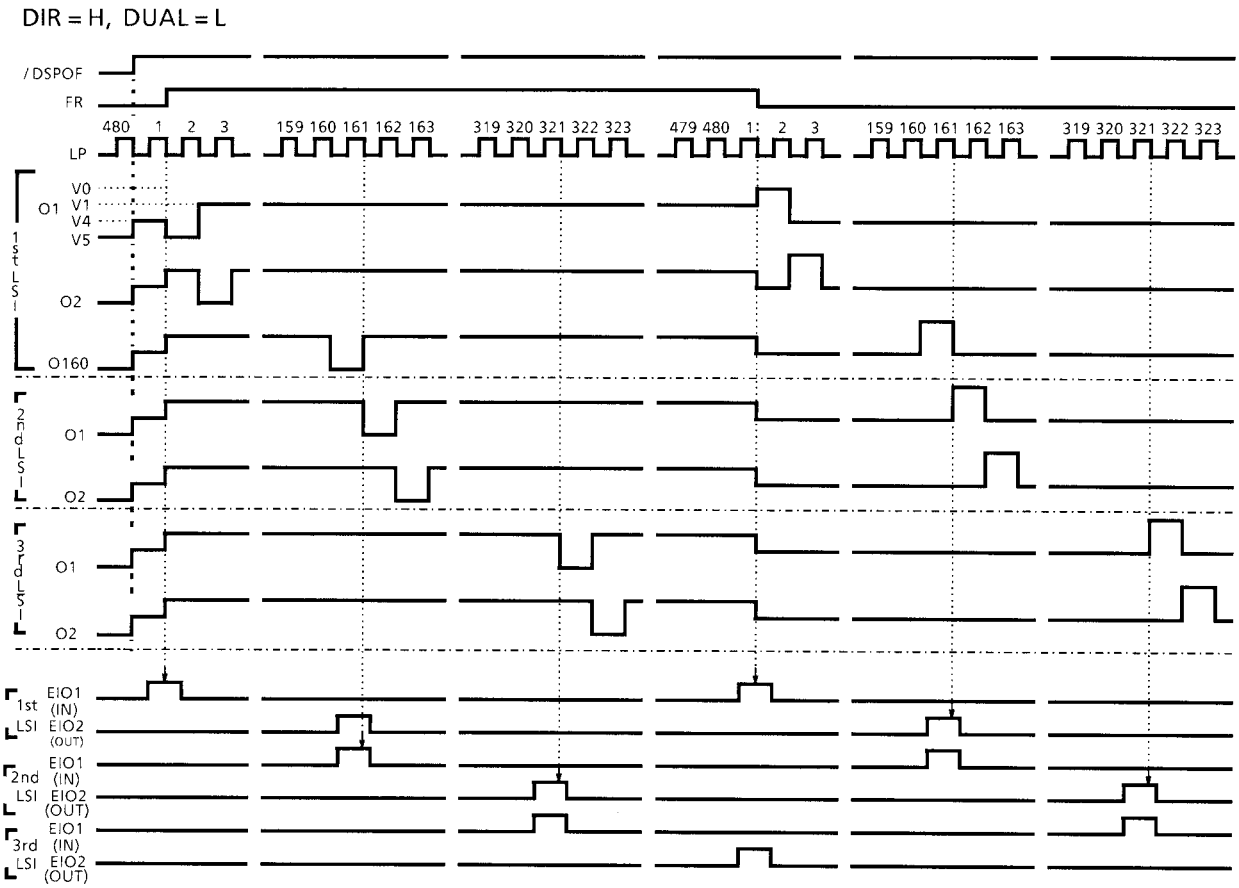
Timing Diagram (Row mode)



Absolute Maximum Ratings
(Ensure that the following conditions are maintained, $V_{CC} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{SS}$)

Item	Symbol	Pin Name	Rating	Unit
Supply Voltage (1)	V_{DD}	V_{DD}	−0.3 to 7.0	V
Supply Voltage (2)	V_{CC}	$V_{CCL / R}$	−0.3 to 45.0	V
Supply Voltage (3)	V_0, V_2	$V_{0L / R}$ $V_{2L / R}$	−0.3 to V_{CC} + 0.3	V
Supply Voltage (4)	V_3, V_5	$V_{3L / R}$ $V_{5L / R}$	−0.3 to 7.0	V
Input Voltage	V_{IN}	(Note 2)	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	—	−20 to 75	°C
Storage Temperature	T_{stg}	—	−40 to 125	°C

Note 2: SCP, FR, LP, DIR, DF, S / C, EIO1, EIO2, DI1 to 8, / DSPOF, TEST

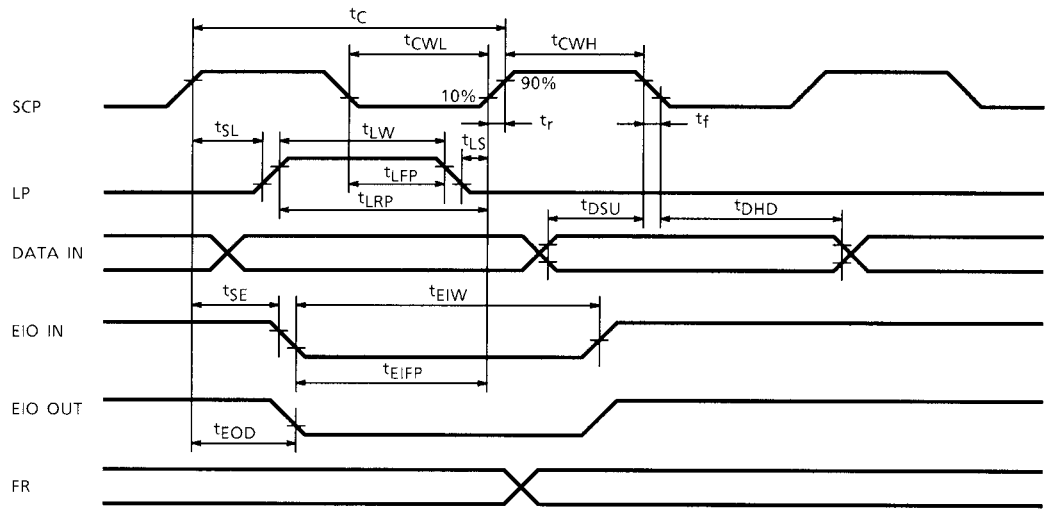
Electrical Characteristics
DC Characteristics
(Unless otherwise noted, V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Ta = −20 to 75°C)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Supply Voltage 1		V_{DD}	—	—	2.7	5.0	5.5	V	V_{DD}
Supply Voltage 2		V_{CC}	—	—	14	—	42		V_{CCL} / R
Input Voltage	H Level	V_{IH}	—	(Note 2)	0.8 V_{DD}	—	V_{DD}		SCP, FR, LP, DIR, DF, S / C, EIO1, EIO2, DI1 to 8, / DSPOF, TEST
	L Level	V_{IL}	—		0	—	0.2 V_{DD}		
Output Voltage	H Level	V_{OH}	—	I_{OH} = − 0.5 mA	V_{DD} − 0.5	—	V_{DD}		EIO1, EIO2
	L Level	V_{OL}	—	I_{OL} = 0.5 mA	0	—	0.5		
Output Resistance	H Level	R_{OH}	—	$V_{OUT} = V_0$ − 0.5 V (Note 3)	—	0.6	1.3	kΩ	O1 to O160
	M Level	R_{OM}	—	$V_{OUT} = V_2$ ± 0.5 V (Note 3)	—	0.6	1.3		
			—	$V_{OUT} = V_3$ ± 0.5 V (Note 3)	—	0.6	1.3		
	L Level	R_{OL}	—	$V_{OUT} = V_5$ + 0.5 V (Note 3)	—	0.6	1.3		
Current Consumption (Note 4)		I_{DD}	—	V_{DD} = 5.5 V V_{CC} = 42 V f_{LP} = 33 kHz f_{FR} = 8.3 kHz f_{scp} = 8.0 MHz Input Data: every bit inverted V_{IH} = 5.5 V, V_{IL} = 0 V	—	—	4.0	mA	V_{DD}

Note 3: V_{CC} = 20 V, 1 / 13 bias

Note 4: Current consumption while the internal data receiver is operating

AC Electrical Characteristics (Column mode)



Test Conditions (1) (V_{SS} = 0 V, V_{DD} = 5 V ± 10%, V_{CC} = 14 to 42 V, Ta = − 20 to 75°C)

Item	Symbol	Test Condition	Min	Max	Unit
Clock Cycle	t_C	—	125	—	ns
SCP Pulse Width	t_{CWH}, t_{CWL}	—	50	—	ns
Data Set−Up Time	t_{DSU}	—	50	—	ns
Data Hold Time	t_{DHD}	—	50	—	ns
SCP Rise / Fall Time	t_r, t_f	—	—	(Note 5)	ns
LP Rise Time	t_{LRP}	—	50	—	ns
LP Fall Time	t_{LFP}	—	50	—	ns
LP Pulse Width	t_{LW}	—	45	—	ns
SCP−to−LP Delay Time	t_{SL}	—	40	—	ns
LP−to−SCP Delay Time	t_{LS}	—	40	—	ns
EIO IN Fall Time	t_{EIFP}	—	40	—	ns
EIO IN Pulse Width	t_{EIW}	—	40	—	ns
SCP−to−EIO Delay Time	t_{SE}	—	20	—	ns
EIO−OUT Delay Time	t_{EOD}	(Note 6)	—	80	ns

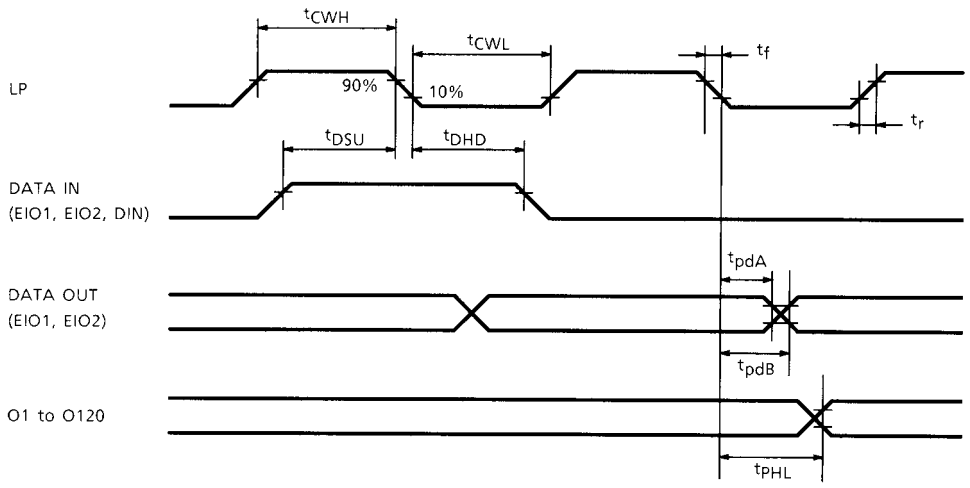
Note 5: t_r, $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and t_r, $t_f \leq 50$ ns
Note 6: C_L = 30 pF

Test Conditions (2) (V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V, V_{CC} = 14 to 42 V, Ta = −20 to 75°C)

Item	Symbol	Test Condition	Min	Max	Unit
Clock Cycle	t_C	—	500	—	ns
SCP Pulse Width	t_{CWH}, t_{CWL}	—	240	—	ns
Data Set−Up Time	t_{DSU}	—	240	—	ns
Data Hold Time	t_{DHD}	—	240	—	ns
SCP Rise / Fall Time	t_r, t_f	—	—	(Note 7)	ns
LP Rise Time	t_{LRP}	—	220	—	ns
LP Fall Time	t_{LFP}	—	240	—	ns
LP Pulse Width	t_{LW}	—	240	—	ns
SCP−to−LP Delay Time	t_{SL}	—	70	—	ns
LP−to−SCP Delay Time	t_{LS}	—	100	—	ns
EIO IN Fall Time	t_{EIFP}	—	240	—	ns
EIO IN Pulse Width	t_{EIW}	—	240	—	ns
SCP−to−EIO Delay Time	t_{SE}	—	50	—	ns
EIO−OUT Delay Time	t_{EOD}	(Note 8)	—	260	ns

Note 7: t_r, $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and t_r, $t_f \leq 50$ ns
Note 8: C_L = 30 pF

AC Electrical Characteristics (Row mode)



Test Conditions (1) (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, V_{CC} = 14 to 42 V, Ta = −20 to 75°C)

Item		Symbol	Test Condition	Min	Max	Unit
LP Pulse Width H		t_{CWH}	LP	30	—	ns
LP Pulse Width L		t_{CWL}	LP	195	—	ns
SCP Rise / Fall Time		t_r, t_f	LP, FR, EIO1, EIO2, DIN	—	20	ns
Data Set−up Time		t_{DSU}	EIO1, EIO2, DIN	80	—	ns
Data Hold Time		t_{DHD}	EIO1, EIO2, DIN	0	—	ns
EIO−OUT Delay Time A	(Note 9)	t_{pdA}	EIO1, EIO2, DIN	5	—	ns
EIO−OUT Delay Time A	(Note 9)	t_{pdB}	EIO1, EIO2, DIN	—	150	ns
LCD Drive Data Delat Time	(Note 10)	t_{PHL}	O1 to O120	—	800	ns

Test Conditions (2) (V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, V_{CC} = 14 to 42 V, Ta = −20 to 75°C)

Item		Symbol	Test Condition	Min	Max	Unit
LP Pulse Width H		t_{CWH}	LP	100	—	ns
LP Pulse Width L		t_{CWL}	LP	400	—	ns
SCP Rise / Fall Time		t_r, t_f	LP, FR, EIO1, EIO2, DIN	—	20	ns
Data Set−up Time		t_{DSU}	EIO1, EIO2, DIN	100	—	ns
Data Hold Time		t_{DHD}	EIO1, EIO2, DIN	0	—	ns
EIO−OUT Delay Time A	(Note 9)	t_{pdA}	EIO1, EIO2, DIN	5	—	ns
EIO−OUT Delay Time A	(Note 9)	t_{pdB}	EIO1, EIO2, DIN	—	400	ns
LCD Drive Data Delat Time	(Note 10)	t_{PHL}	O1 to O120	—	1000	ns

Note 9: C_L = 30 pF
Note 10: C_L = 20 pF

Note: Insert the bypass capacitor (0.1 μF) between V_{DD} and V_{SS}, to decrease power supply noise.
Place the bypass capacitor as close to the LSI as possible.

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